The Dissertation Committee for Chengqing Hu Certifies that this is the approved version of the following dissertation:

Nanoelectronics Based on Epitaxial Oxides

Committee:

Edward T. Yu, Supervisor

Jack C. Lee

Leonard F. Register

John G. Ekerdt

Nan Sun

Nanoelectronics Based on Epitaxial Oxides

by

Chengqing Hu, B.S.; M.S.E.

Dissertation

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Doctor of Philosophy

The University of Texas at Austin

August 2015

Dedication

To my parents, Fengxiang Hu and Shuping Qian

Acknowledgements

It is a pleasure to sincerely acknowledge my advisor, Professor Edward T. Yu, for his consistent guidance, support, and concern throughout my years of graduate study. My graduate research and career development have benefited immensely from his insight into the methodology of scientific research, dedication to solving practical engineering problems, and excellence in managing his laboratory. I am also grateful for his concern for my personal well-being and enlightening advice for my career growth.

I would like to express my gratitude to Professor John G. Ekerdt and Professor Alexander A. Demkov for the collaborations and interactions during my graduate study. Their knowledge and understanding in advanced thin-film oxide deposition techniques as well as the facilities in their laboratories capable of producing high-quality epitaxial oxides have greatly fueled my research presented in this dissertation. I have also benefited from some fascinating conversations with Professor Leonard F. Register, Professor Nan Sun, Professor Hao Ling, and Professor Maxim Tsoi, who have provided valuable advice regarding the various aspects of my research projects. The X-ray diffraction images from Dr. Jean L. Jordan-Sweet of IBM Thomas J. Watson Research Center contributed substantially to the success and quality of the $LaCoO_3/SrTiO_3$ studies reported in this dissertation. I would also like to thank Professor Jack C. Lee for serving on the committee for my qualifying examination and dissertation.

I am grateful for having had the privilege to work and interact with my colleagues at the University of Texas at Austin. I am indebted to Dr. Lei Zhu for leading me into the world of spintronics and for his patience and generosity in teaching me about many laboratory skills. My understanding and skills in scanning probe microscopy have

profited significantly from Dr. Keun Woo Park who has extraordinary expertise in the field. I have enjoyed a number of fruitful collaborations with Dr. Martin D. McDaniel and Dr. Agham Posadas, from which I obtained high-quality epitaxial oxide samples for my device research and extracted considerable knowledge about materials physics, growth, and characterization techniques of oxide thin films. I have enjoyed my interactions, both scientific and recreational, with Aiting Jiang, who is knowledgeable in many aspects. I have learnt a great deal from my interactions with Dr. Hosung Seo, Stefano Larentis, Dr. Ping-Chun Li, Heng-Lu Chang, Shen Hu, and Fei Zhou. My life in Austin has been enriched by my friends previously or currently at the Microelectronics Research Center, Dr. Jingsi Li, Feng Lu, Dr. Xiaochuan Xu, Dr. Xiaohui Lin, Danlu Wang, Hui Dong, Yao-Feng Chang, Mingzhou Jin, Dr. Li Tao, Zhongjian Zhang, Dr. Rodolfo Salas, and Dr. Wei-Cheng Lai. I wish them all the best.

Finally, I would like to thank my parents for their love, encouragement, and support. My parents have always encouraged me to define and pursue worthwhile goals with steadiness and a spirit of dedication to our society. Without my parents none of this work would have been possible, and this dissertation is dedicated to them, my dearest parents.

Nanoelectronics Based on Epitaxial Oxides

Chengqing Hu, Ph.D.

The University of Texas at Austin, 2015

Supervisor: Edward T. Yu

Crystalline oxide materials and heterostructures have been under extensive investigation owing to the richness of the physical, chemical, and electrical properties they exhibit, including ferromagnetism, ferroelectricity, ferrotoroidicity, superconductivity, metal-insulator transition, multiferroics, and 2-dimensional electron liquids. In recent years, the advancement of thin film growth techniques such as molecular beam epitaxy and atomic layer deposition has made possible monolithic integration of these crystalline oxide materials with mainstream semiconductor substrate materials such as Si and Ge, which opens new avenues for improving existing device performance and provides many opportunities for adding various solid-state device functionalities to electronic devices that are unachievable with conventional semiconductor materials.

Epitaxial oxide heterostructures with a perovskite crystal structure are emerging as outstanding candidates for realization of devices in which diverse material properties - ferromagnetism, piezoelectricity, ferroelectricity, and others - are flexibly coupled to achieve new functionality. In the first part of this dissertation, the strain-dependent ferromagnetism in $LaCoO_3$, piezoelectric response in $SrTiO_3$, and their strain coupling in a single-crystal oxide heterostructure grown on Si (001) are employed to enable a novel

approach to modulating ferromagnetism and magnetoresistance by application of a gate voltage in a suitably fabricated device.

The second part of the dissertation addresses the resistive switching behavior and physics of epitaxial single-crystal anatase TiO_2 on silicon and demonstrates several unique advantages of using single-crystal metal oxide films as an active switching layer, including a high ON/OFF ratio, a great potential for device scaling, highly linear current-voltage characteristics, and room-temperature, reproducible quantization of conductance, etc.

Finally, epitaxial $SrHfO_3$-based gate stacks for Ge metal-oxide-semiconductor devices are investigated as an approach to alleviate the gate dielectric interface quality problem that has tremendously hampered the adoption of next-generation Ge-based transistors. Different methods are shown to effectively decrease the interface trap density, and the gate stacks developed in this dissertation represent the state of the art in terms of the combination of equivalent oxide thickness and gate leakage.

In summary, this dissertation presents several results in the design and modeling, process integration, characterization, and analysis of device prototypes for functional and nano- electronics applications using epitaxial oxide films. These results provide a foundation for further exploration of solid-state device applications using epitaxial crystalline oxide materials.

Table of Contents

List of Tables

List of Figures

Figure 2.4: (a) Cross-sectional view of device geometry and contact configuration for finite-element modeling of electric field distribution. Simulation results of the circumscribed region are shown in (c). (b) Channel current vs. V_C at 77 K with $H = 4.5$ kOe for (i) $V_{G1} = 0$ V, $V_{G2} = 0$ V; (ii) $V_{G1} = +15$ V, $V_{G2} = 0$ V; (iii) $V_{G1} = 0$ V, $V_{G2} = +15$ V; and (iv) $V_{G1} = +15$ V, $V_{G2} = +15$ V. Different gate biasing configurations lead to different electric field distributions and therefore variations in modulation of strain in the $SrTiO_3$ layer, and of ferromagnetism in the $LaCoO_3$ layer. (c) Finite element simulations of electric field (vertical component) distributions in the $SrTiO_3$ layer for gate voltage applied in different configurations. In the first two cases where +15 V is applied to either set of gate fingers, well-defined unbiased regions in the $SrTiO_3$ layer can be found. In the third case, fringing fields at the gate contact edges penetrate the unbiased region, leading to laterally extended modulation in electric field and consequently strain. This expansion in electric field modulation results in reduced modulation of channel current in the case of $V_{G1} = V_{G2} = +15$ V. (d) Schematic diagram (left) and truth table (right) for a two-input exclusive-NOR (XNOR) logic gate implemented by our device structure. High (low) voltage is defined as 1 (0) for both inputs and output so that $Y = V_{G1} \odot V_{G2}$.....21

Chapter 1: Introduction

1.1 Research Background

Metal oxides are a class of materials that exhibit a broad range of interesting electronic, magnetic, optical, and chemical properties that are not only of fundamental scientific importance, but also offer rich possibilities for exploration of device applications that are unattainable with conventional semiconductor materials. Due to the inherent complexities of orbital, charge, and spin states of these oxide materials, differences in metal cations, phases, composition, and stoichiometry can change an oxide material from electrically insulating to semiconducting to superconducting, from paraelectric to piezoelectric to ferroelectric, from low-κ to high-κ, from narrow bandgap to wide bandgap, from paramagnetic to ferromagnetic to antiferromagnetic, or from chemically reactive to inert. These useful properties and the flexibility of changing them by applying appropriate synthesis, growth, or fabrication process conditions enable metal oxides to be widely used in a variety of applications, including electronics, energy, medical devices, and others.

In recent years, monolithic integration of crystalline oxide heterostructures has been made possible with the advancement of thin film growth techniques such as molecular beam epitaxy (MBE), pulsed laser deposition, and atomic layer deposition (ALD). [1] Compared with their single-layer counterparts, epitaxial oxide heterostructures offer more degrees of freedom for integrating novel functionalities into conventional electronic devices and can even create exotic and unpredicted properties that cannot be achieved with a single oxide material. An outstanding example is the discovery of a high carrier density 2-dimensional electron liquid (2DEL) at the $SrTiO_3/LaAlO_3$ heterointerface. [2] It has been found that due to the polarization

discontinuities resulting from the incomplete atomic coordinations, a 2DEL emerges at the interface of TiO_2-terminated $SrTiO_3$ and $LaAlO_3$ as a result of electronic reconstruction, creating an electron-doped conducting channel between these two insulating materials. By contrast, no emergent phenomena were found at the interface of SrO-terminated $SrTiO_3$ and $LaAlO_3$ due to ionic compensation, and the hole-doped channel at the interface is therefore insulating. Another topic of intense current interest employing epitaxial heterostructures lies in the development of magnetic and electronic coupling between two adjacent layers, by which electrical control of magnetic properties or magnetic control of electrical properties can be achieved for sensing applications. [3]

Oxygen vacancies and their influence on the physical, chemical, and electrical properties has been another subject that attracts intense theoretical and experimental interest. [4] In most cases, oxygen vacancies can easily be induced by adjusting the oxygen atom flux or the precursor cycling ratio during growth or by heating the as-grown sample in an appropriate atmosphere (e.g., ultra high vacuum). Among the various transition metal oxides in which such behavior has been investigated, TiO_2 is by far the most widely investigated oxide material for this topic. As the number of oxygen vacancies in TiO_2 increases, more Ti^{4+} ions are reduced and become donors, leading to localized states which, depending on the detailed donor level, can contribute electrons to the conduction band and make TiO_2 n-doped. Titanium oxide is also well known for its rich phases and suboxide phases that result in a complex phase diagram, with different phases exhibiting widely varying electrical conductivity.

Because of the possibility of controlling the electrical conductivity via the concentration and distribution of oxygen vacancies, TiO_2 is also one of the most studied materials for resistive switching (RS) applications. [5] Despite the diverse switching behaviors (bipolar and unipolar) observed in TiO_2 systems and the proposed detailed

switching mechanisms (filamentary, interfacial, thermochemical, and redox-based) that are sometimes contradictory to each other, [5] oxygen vacancies are nevertheless believed to play a crucial role in driving these switching processes. In this context, owing to the nearly perfect crystal structure and therefore minimized oxygen vacancy background in pristine devices, single-crystal epitaxial TiO_2 thin films can provide valuable information for revealing the physical nature of oxygen vacancy dynamics as being responsible for the RS behavior, and are shown in this dissertation to exhibit switching characteristics that differ dramatically from those observed in other forms of TiO_2.

Finally, epitaxial oxides can also be promising candidates for application as gate dielectrics for Ge-based field-effect transistors, for which the development has been largely hampered by the poor quality gate dielectric/channel interface. It has been reported that epitaxial oxides grown on Ge enable the formation of commensurate interface structures while maintaining continuity in dielectric displacement and systematic control of inversion charge, [6] based on which a high-mobility metal-oxide-semiconductor field-effect transistor (MOSFET) can be made. In this dissertation, we show that epitaxial $SrHfO_3$ stands out as a particularly promising option owing to its very small lattice mismatch with Ge, excellent crystallinity enabled by direct ALD growth on the Ge surface, and favorable electronic properties as a high-κ oxide.

1.2 Dissertation Outline

This dissertation centers on the applications of epitaxial oxides for functional and nano- electronics, and encompasses design and modeling, process integration, characterization, and analysis of device prototypes using epitaxial oxides. The work of this dissertation includes the following three parts.

In Chapter 2, a $LaCoO_3/SrTiO_3$ heterostructure grown on Si (001) is shown to provide electrically switchable ferromagnetism, a large, electrically tunable magnetoresistance, and a vehicle for achieving and probing electrical control over ferromagnetic behavior at submicron dimensions. Fabrication of devices in a field-effect transistor geometry enables application of a gate bias voltage that modulates strain in the heterostructure via the converse piezoelectric effect in $SrTiO_3$, leading to an artificial inverse magnetoelectric effect arising from the dependence of ferromagnetism in the $LaCoO_3$ layer on strain. Below the Curie temperature of the $LaCoO_3$ layer, this effect leads to modulation of resistance in $LaCoO_3$ as large as 100%, and magnetoresistance as high as 80%, both of which arise from carrier scattering at ferromagnetic-nonmagnetic interfaces in $LaCoO_3$. Finite-element numerical modeling of electric field distributions is used to explain the dependence of carrier transport behavior on gate contact geometry, and a Valet-Fert transport model enables determination of spin polarization in the $LaCoO_3$ layer. Piezoresponse force microscopy (PFM) is used to confirm the existence of piezoelectric response in $SrTiO_3$ grown on Si (001).

Chapter 3 demonstrates the use of single-crystal anatase-TiO_2 thin films epitaxially grown on silicon by ALD for RS applications. Highly stable and clean bipolar resistive switching (BRS) behavior with a record high ON/OFF ratio ($\sim 10^7$) and extremely low leakage current in the high-resistance state (HRS) are observed. We demonstrate that although the valence change mechanism is responsible for the observed RS, single-crystal anatase-TiO_2 thin films show electrical characteristics that are very different from the usual switching behaviors observed for polycrystalline or amorphous TiO_2 and instead very similar to those found in electrochemical metallization memory. In addition, we demonstrate highly reproducible quantized conductance (QC) that is well controlled by application of a compliance current and that suggests the localized

formation of conducting Magnéli-like nanophases. The QC observed results in multiple well-defined resistance states suitable for implementation of multilevel memory cells. A physics-based analytical model is presented to systematically explain the SET and RESET processes and is verified to be consistent with the electrical characteristics that we have observed experimentally and that are fundamentally different from what have been reported in literature.

Chapter 4 demonstrates and presents detailed electrical characterization of a high-κ epitaxial oxide gate stack based on crystalline $SrHfO_3$ grown on Ge (001) by ALD. We developed metal-oxide-Ge capacitor structures that show extremely low gate leakage, small and scalable equivalent oxide thickness, and good and reducible interface trap density (D_{it}). Detailed growth strategies and post-growth annealing schemes are employed to reduce D_{it}. The physical mechanisms behind these phenomena are studied, and suggest approaches for further reduction of D_{it}.

Chapter 5 summarizes the work demonstrated in this dissertation, and proposes potential future directions for exploration.

Chapter 2: Voltage-Controlled Ferromagnetism and Magnetoresistance in $LaCoO_3/SrTiO_3$ Heterostructures[1]

2.1 INTRODUCTION

Complex oxide materials and heterostructures have excited tremendous interest in research due to the wealth of new physical phenomena they exhibit and their potential for producing solid-state device functionality unattainable with conventional semiconductor materials. In particular, multiferroic and other multifunctional oxide materials offer rich possibilities for exploration of both fundamental physical phenomena and device applications, [3, 7–18] and with the advancement of thin film growth techniques for such oxide materials, epitaxial oxide heterostructures are emerging as outstanding candidates for realization of devices in which diverse material properties – ferromagnetism, piezoelectricity, ferroelectricity, and others – are flexibly coupled to achieve new functionality.

Among various possibilities for combining electronic, magnetic, or other functionalities, electric-field control of magnetism has piqued particularly intense interest, and may provide an attractive alternative to approaches such as current-induced spin-transfer torque for low-power magnetization switching. Electric-field modulation of magnetization direction, saturation magnetization, or coercive field has previously been demonstrated, [19–43] as have switching between ferromagnetic and paramagnetic states via modulation of carrier concentration in itinerant magnetic materials, generally using a

[1] Content of Chapter 2 has been published as C. Hu, K. W. Park, A. Posadas, J. L. Jordan-Sweet, A. A. Demkov, and E. T. Yu, "Voltage-controlled ferromagnetism and magnetoresistance in $LaCoO_3/SrTiO_3$ heterostructures", *J. Appl. Phys.* **114**, 183909 (2013). C. Hu designed, modeled, fabricated, characterized, and analyzed the devices involved in this work. K. W. Park contributed to the piezoresponse force microscopy studies. A. Posadas and A. A. Demkov contributed to the epitaxial growth of the $LaCoO_3/SrTiO_3$ heterostructures. J. L. Jordan-Sweet contributed to the X-ray diffraction studies. E. T. Yu supervised the work in every aspect. All the authors contributed to the writing and revision of the manuscript.

liquid electrolyte as a gate contact, [44–48] and macroscopic control over interfacial magnetocrystalline anisotropy in a multiferroic epitaxial heterostructure. [49, 50] However, practical device structures making use of electric-field switching of ferromagnetism that remain amenable to on-chip integration with established Si and Si-based electronics and device size scaling are still lacking.

In the work described in this chapter, we have employed an approach that combines strain-dependent ferromagnetism in $LaCoO_3$ [51–58] with piezoelectric response in $SrTiO_3$ [25, 59–62] in a single-crystal oxide heterostructure grown on Si (001) to enable application of a gate voltage in a suitably fabricated device to modulate strain in both the $SrTiO_3$ and $LaCoO_3$, and consequently ferromagnetism in the $LaCoO_3$ layer. Creation of spatially alternating ferromagnetic and nonmagnetic regions in a $LaCoO_3$ film in this manner leads to a voltage-dependent magnetoresistance, [63] and engineering of the strain distribution within the $LaCoO_3/SrTiO_3$ heterostructure enables realization of exclusive-NOR logic functionality within a single device. In addition, monolithic integration on Si (001) via epitaxial growth offers the possibility of incorporating these and related devices into mainstream Si-based nanoelectronic circuits and systems.

2.2 Experimental Details

The epitaxial layer structures employed in these studies were grown by MBE (DCA M600) from elemental sources and consisted of 8 nm $SrTiO_3$ grown on a p-type Si (001) ($\rho \sim 0.01\ \Omega$ cm) substrate, followed by 30 nm $LaCoO_3$ [52]. Prior to growth, the Si substrates were degreased in acetone, isopropanol, and deionized water for 5 min each with sonication. The substrates were then exposed to ultraviolet/ozone for 15 min to volatilize hydrocarbon impurities. After loading into the MBE chamber, the Si was

outgassed for 10 min at 650 °C and the native SiO_2 layer was removed by Sr-assisted deoxidation [64]. $SrTiO_3$ was grown on Si using a ½ monolayer Sr template [65] with the metal fluxes adjusted to yield a total growth rate of 0.4 nm/min. The first 1.6 nm were grown at 200 °C and vacuum annealed at 550 °C for 5 min. The rest of the $SrTiO_3$ layer was grown at 550 °C to achieve a total thickness of 8 nm. $SrTiO_3$ growth was done using molecular oxygen as the oxidant at a partial pressure of 2×10^{-7} torr. After $SrTiO_3$ growth, the substrate temperature was raised to 700 °C while the atomic oxygen rf plasma source power was being ramped up. $LaCoO_3$ was grown under atomic oxygen (rf power 300 W and oxygen background pressure of 1×10^{-5} torr) at a growth rate of 0.6 nm/min to a total thickness of 30 nm. After growth, the sample was cooled down to room temperature in oxygen (1×10^{-5} torr) at a rate of 10 °C/min. High temperature growth of the $LaCoO_3$ layer under atomic oxygen also results in formation of ~8.5 nm SiO_2 between the Si and $SrTiO_3$, which relaxes compressive strain in $SrTiO_3$ on Si [66] and provides additional tensile strain in $LaCoO_3$ that helps stabilize ferromagnetism in that layer, and also isolates the active device region from the conducting Si substrate. To fabricate the device structures shown schematically in Figure 2.1(a), electrical contacts to the $LaCoO_3$ layer were formed by initial deposition of 25 nm SiO_2, followed by e-beam lithography and etching of 4 μm × 2.5 μm contact windows and deposition of Ti/Au contact metallization. The typical length of the $LaCoO_3$ channel formed in this manner was 13 μm for M = 9 and 26 μm for M = 18. For each device, two Ti/Au gate contacts were formed on the SiO_2 layer above the channel in an alternating finger pattern by e-beam lithography, e-beam evaporation and lift-off. The finger widths for the two gate contacts are 500 nm and 200 nm, with adjacent fingers separated by 150 nm. A Carl Zeiss Neon 40 scanning electron microscope was used to obtain the images shown in Figure 2.1(b).

X-ray diffraction was performed at the National Synchrotron Light Source beamline X20A using a high resolution triple-axis geometry with a Ge (111) monochromator and analyzer. The x-ray wavelength was 1.5407 Å and the incident beam divergence was ~0.01 degrees. Grazing incidence and reflection scans were measured for the determination of in-plane lattice parameters at an angle of $\alpha = \beta = 0.4$ degrees to the sample surface, along both the h00 and hk0 directions. Out-of-plane lattice parameters were measured from Bragg-Brentano scans through the 00l peaks. Rocking curves were also taken to determine the FWHM of epitaxial alignment.

All the electrical measurements were performed in a LakeShore EMPX-HF probe station with a high vacuum (10^{-6} mbar) chamber. Liquid nitrogen was used for low temperature measurements. An Agilent 4156A precision semiconductor parameter analyzer was used for applying a channel bias voltage and measuring electrical currents; an Agilent B2912A precision source/measure unit was used to apply a gate bias voltage. The temperature dependence of the $LaCoO_3$ resistivity was determined by using standard four-probe measurements in which one port from the Agilent B2912A precision source/measure unit was connected as a current source providing 1 nA – 400 μA of current (depending on temperature) between the two end contacts of a standard four-contact device designed and fabricated specifically for four-probe measurements and the other port connected to the two middle contacts across which the voltage drop was measured. For magnetic field sweep measurements, the magnetic field was first swept from 0 Oe to +5 kOe (–5 kOe) with $V_{G1} = +15$ V, followed by resetting V_{G1} and H successively and then a second field sweep from 0 Oe to +5 kOe (–5 kOe).

The electrostatic module from Comsol Multiphysics was used for the finite element modeling and simulations. A gate bias voltage of 15 V was applied as a

boundary condition at locations corresponding to the gate contacts. The Si substrate was assumed to form a conductive plane in the simulation since it was heavily doped. Relative dielectric constants used were 3.9 for SiO_2, 1000 for $LaCoO_3$ (estimated based on Huang *et al*. [67]) without considering the rather limited electric field screening by the carriers in the $LaCoO_3$, and 300 for $SrTiO_3$. [68, 69]

PFM measurements were performed at room temperature using a Bruker ICON atomic force microscope system with a Co/Cr coated MESP-tip in contact mode. PFM images were obtained with 4.5 V amplitude, 8 kHz ac voltage modulation at 0 V dc bias and the setpoint was minimized to prevent excessive wearing of the tip coating. The system has two lock-in amplifiers which detect the same frequency component of the four-quadrant photodiode detector as that of the applied electric field, one for the horizontal and the other for the vertical deflections.

2.3 Results and Discussion

Figure 2.1(a) shows a schematic diagram of a completed device structure along with electrical contact and external field geometries, with scanning electron micrographs of a representative device structure shown in Figure 2.1(b). The 8.5 nm SiO_2 layer indicated in Figure 2.1(a) forms during the growth of $LaCoO_3$, which requires high temperature (700 °C) and the use of atomic oxygen from an oxygen plasma source. The oxidation of the Si after $SrTiO_3$ growth does not disrupt the crystalline structure of the $SrTiO_3$ layer away from the SiO_2, allowing for subsequent epitaxial growth of $LaCoO_3$, [66] and relieving strain induced by the Si substrate in the $SrTiO_3$. Minimal intermixing at the $LaCoO_3/SrTiO_3$ interface is expected under these conditions. [52] The basic device geometry is that of a field-effect transistor in which the $LaCoO_3$ layer acts as the

transistor channel, with source-drain voltage V_C and dual gate contacts with voltages V_{G1} and V_{G2} applied.

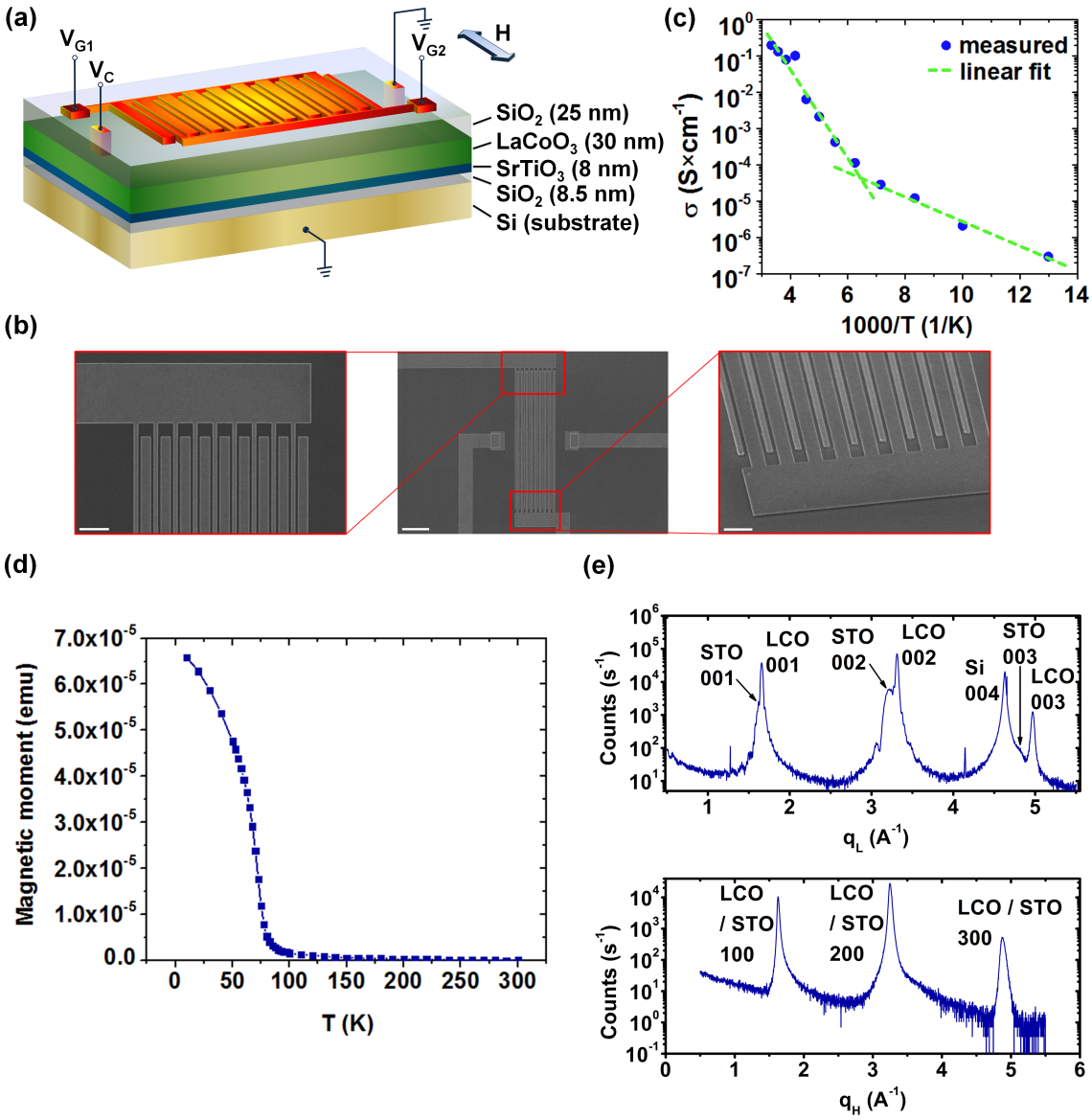


Figure 2.1.

Figure 2.1: (a) Schematic diagram of device structure, applied voltages, and external magnetic field geometry. (b) Conductivity of the $LaCoO_3$ channel measured as a function of temperature ranging from 77 K to 300 K. Two distinct slopes are observed in different temperature ranges (77 K to 150 K and 150 K to 300 K) indicating two different regimes of electronic transport. (c) SEM images of device. Scale bars from left to right are 1.5 μm, 6 μm, and 1 μm, respectively. (d) Magnetization of $LaCoO_3$ as a function of temperature at a constant magnetic field of 1 kOe under field-cooled conditions. The film is ferromagnetic with a Curie temperature of 85 K. (e) X-ray diffraction data of $LaCoO_3$ (30 nm)/$SrTiO_3$ (8 nm)/SiO_2 (8.5 nm)/Si. The $LaCoO_3$ peaks are indexed using the pseudocubic notation. The data shows that $LaCoO_3$ and $SrTiO_3$ are coherently strained to each other, and they are indeed epitaxially grown on Si.

Figure 2.1(c) shows temperature-dependent channel conductivity, measured using a standard four-probe method under zero external magnetic field. Two temperature regimes, 77 K – 150 K and 150 K – 300 K, both showing an Arrhenius or Arrhenius-like relation, can be seen with different activation energies, respectively, providing insight into the temperature-dependent electrical transport in thin-film single-crystalline $LaCoO_3$. It is known that polaronic conduction plays an important role in electrical transport in many strongly correlated oxides. This has been observed for bulk $LaCoO_3$, in which small polarons are formed by mobile holes in the valence band due to electron thermal excitation whereas electrons are deeply trapped and therefore immobile. [70] The small-polaron motion is known to occur by two distinct mechanisms. [71, 72] At low temperatures, the small polaron moves by Bloch-type band motion and the temperature dependence of the dc conductivity is given as $\sigma = e\mu_{\mathrm{low\,T}} n_0 \exp\left(-E_g/2k_B T\right)$, where e denotes the electronic charge, n_0 is the number of low-spin Co(III) sites per unit volume at very low temperatures, $\mu_{\mathrm{low\,T}}$ is the mobility of small-polarons at low temperatures (slowly depending on T as for conventional semiconductors), and E_g is the quasi-constant band gap of $LaCoO_3$. In this regime, the small-polaron transport can be described in a conventional way widely used for most semiconductors. At high temperatures, however, thermally-activated phonon-induced small-polaron hopping dominates and the conductivity-temperature relation is expressed as $\sigma T = A_0 \exp\left[-\left(W_H + E_g/2\right)/k_B T\right]$, where A_0 is a constant, W_H is the hopping energy of a polaron, and the small-polaron hopping mobility is exponentially depending on $1/T$. The $\sigma - T$ data obtained in our work for the $LaCoO_3$ thin film are in accord with this theory, from which E_g and W_H are estimated to be 0.14 eV and 0.19 eV, respectively, close to those reported by Iguchi *et al*. [70] Therefore, as described below, the Valet-Fert model derived from the Boltzmann

equation can be used to describe electrical transport in the $LaCoO_3$ film at temperatures below 150 K. [63]

The magnetic properties of the $LaCoO_3$ were measured using a Quantum Design superconducting quantum interference device (SQUID) magnetometer. The magnetization as a function of temperature from 300 K to 10 K was measured under an applied field of 1 kOe in a field-cooled condition, after the film was first saturated at 10 K under a field of 40 kOe. The field was applied in the plane of the film. Figure 2.1(d) shows the ferromagnetic transition temperature of 85 K for the strained $LaCoO_3$ in our study. The $LaCoO_3$ film was also characterized using x-ray diffraction (XRD) to determine the lattice constants and overall crystalline quality (Figure 2.1(e)). The *c* lattice constants of the $LaCoO_3$ layer and the underlying $SrTiO_3$ layer are determined to be 3.79 Å and 3.91 Å, respectively, whereas the *a* (in-plane) lattice constants of the two layers are both 3.87 Å, consistent with biaxially tensile-strained $LaCoO_3$ with an in-plane lattice constant identical to that of the $SrTiO_3$. Excellent crystalline quality of the $LaCoO_3$ layer as well as the $SrTiO_3$ layer is evident from both Figure 2.1(e) and the results of the transmission electron microscopy as well as the x-ray photoelectron spectroscopy measurements of the same structure. [52] The observation of coherent strain in $LaCoO_3$ thin films at such a large thickness (30 nm) has also been reported by Fuchs *et al*. [73] and is known to be anomalously large compared to the expected critical thickness from the Blakeslee formula. This has been attributed to the existence of nanotwins in $LaCoO_3$ that accommodate the strain without elastic relaxation.

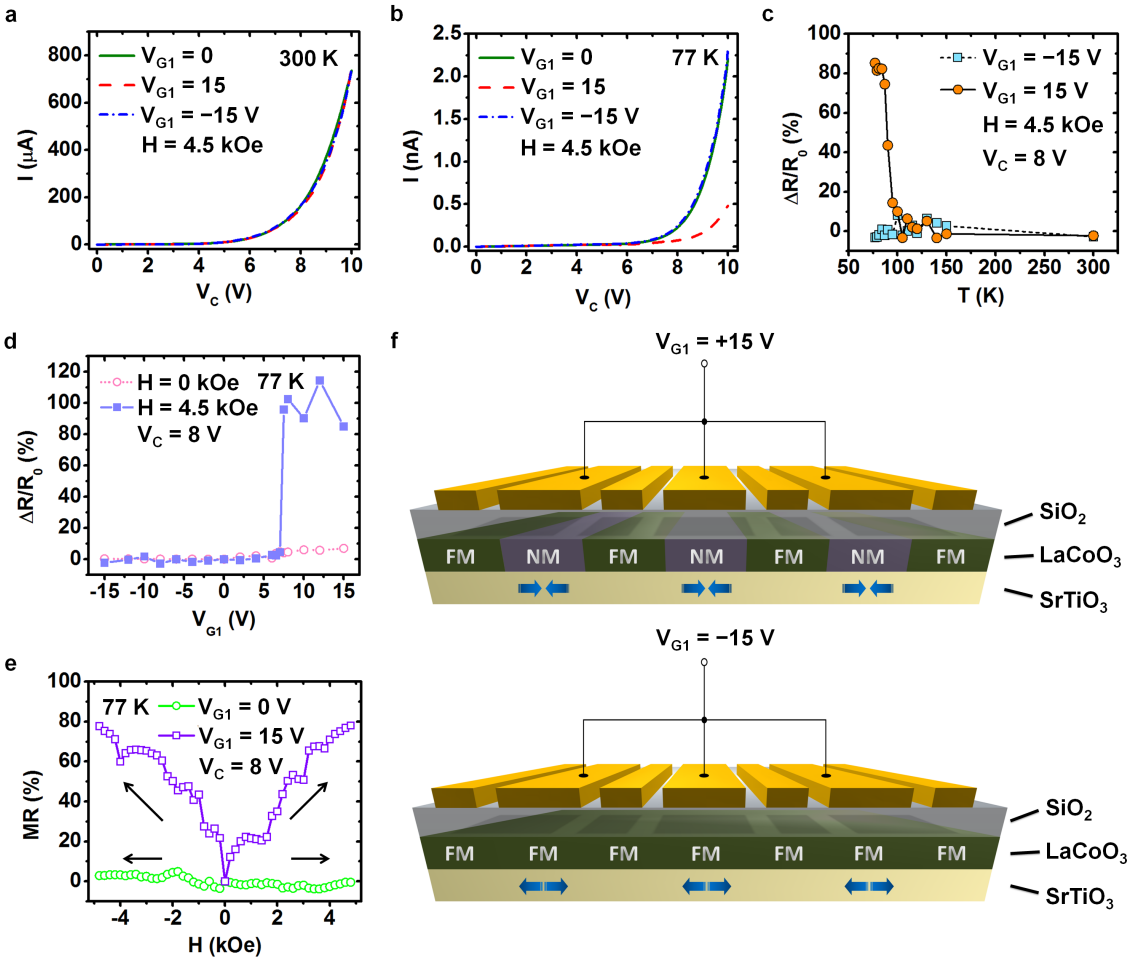

a
b
c
d
e
f
300 K
77 K
V_{G1} = 0
V_{G1} = 15
V_{G1} = −15 V
H = 4.5 kOe
V_C = 8 V
I (μA)
I (nA)
V_C (V)
ΔR/R$_0$ (%)
T (K)
H = 0 kOe
V_{G1} (V)
MR (%)
H (kOe)
V_{G1} = +15 V
V_{G1} = −15 V
FM
NM
SiO_2
$LaCoO_3$
$SrTiO_3$

Figure 2.2.

Figure 2.2: (a) Channel current I vs. channel voltage V_C at 300 K with $H = 4.5$ kOe for gate voltages $V_{G1} = -15$ V, 0 V, and +15 V. V_{G1} is seen to have no effect on channel current flow. (b) Channel current vs. V_C at 77 K with $H = 4.5$ kOe for $V_{G1} = -15$ V, 0 V, and +15 V. Channel current is strongly suppressed for $V_{G1} = +15$ V. (c) $\Delta R / R_0$ vs. T for $V_C = 8$ V and $H = 4.5$ kOe at $V_{G1} = +15$ V and $V_{G1} = -15$ V. Nonzero $\Delta R / R_0$ is observed only for $V_{G1} = +15$ V, and only below the Curie temperature of the $LaCoO_3$ layer. (d) $\Delta R / R_0$ vs. V_{G1} for $V_C = 8$ V at 77 K with/without an external magnetic field H. Negligible change in resistance is observed in the absence of an external magnetic field. For $H = 4.5$ kOe, an abrupt transition in $\Delta R / R_0$ is observed at $V_{G1} = 7.5$ V. (e) MR vs. external magnetic field H for $V_C = 8$ V at 77 K, and gate bias voltages $V_{G1} = 0$ V, +15 V. Magnetic field was first swept from 0 Oe to +5 kOe (−5 kOe) with $V_{G1} = +15$ V, followed by resetting V_{G1} and H successively and then a second field sweep from 0 Oe to +5 kOe (−5 kOe). (f) Illustration of the postulated materials response to $V_{G1} = +15$ V and −15 V, respectively. $V_{G1} = +15$ V results in lateral compression of the $SrTiO_3$ layer below the fingers followed by a ferromagnetic-nonmagnetic transition of $LaCoO_3$ in these regions, whereas $V_{G1} = -15$ V increases tensile strain in the $SrTiO_3$ layer and the $LaCoO_3$ layer atop remains ferromagnetic.

Figure 2.2(a) and (b) shows channel current I measured as a function of V_C for different gate voltages V_{G1}, at 300 K and 77 K, respectively, with V_{G2} = 0 V and an external magnetic field of 4.5 kOe applied in all cases. The I-V_C curves are nonlinear throughout the entire channel bias range, indicating the presence of Schottky contacts to the $LaCoO_3$ channel and leading to a contact resistance that is voltage dependent. I is seen to be independent of V_{G1} at 300 K, but to be strongly suppressed for V_{G1} = +15 V at 77 K. Furthermore, a +15 V bias was applied to either set of gate fingers with 0 V channel bias at 77 K, and the measured current at either end of the channel was smaller than 50 pA (not shown), so the possibility of any contribution by a gate leakage current to the observed current suppression can be eliminated.

We can define a normalized resistance change,

$$\Delta R/R_0 \equiv \left(R|_{V_{G1}} - R|_{V_{G1}=0}\right)/R|_{V_{G1}=0} \quad , \tag{2.1}$$

as a function of V_{G1}, where $R \equiv V_C / I$ is the channel resistance. Here, R contains both the total contact resistance R_c and the $LaCoO_3$ channel resistance $R_{channel}$. To compare and analyze $R_{channel}$ under different conditions, we use a fixed channel voltage V_C = 8 V, in which case R_c is fixed and relatively small, and makes a negligible contribution to the resistance change. Figure 2.2(c) shows $\Delta R / R_0$ as a function of temperature for V_{G1} = −15 V and V_{G1} = +15 V, with V_C = 8 V in all cases. For V_{G1} = +15 V, there is a sharp drop in $\Delta R / R_0$ between 80 K and 90 K, with negligible dependence on temperature observed above 100 K. This transition coincides in temperature with the measured Curie temperature of strained $LaCoO_3$ of ~85 K, [52] suggesting a connection between the electrical behavior shown in Figure 2.2(b) and (c) and ferromagnetism in the $LaCoO_3$ layer. Further evidence suggesting such a connection can be seen in Figure 2.2(d), which shows $\Delta R / R_0$ as a function of V_{G1} at 77 K for V_C = 8 V and external magnetic fields of 0 and 4.5 kOe. Two features are of particular interest. First, no dependence of channel

resistance on V_{G1} is observed in the absence of an applied magnetic field, indicating that magnetic-field-dependent transport plays a significant role. Second, in the presence of an external magnetic field the channel resistance increases very abruptly at V_{G1} = 7.5 V, indicative of an abrupt change in magnetotransport behavior at that voltage. We define magnetoresistance in the channel of the device to be given by

$$MR \equiv (R|_H - R|_{H=0})/R|_{H=0} \quad , \quad (2.2)$$

where R is again the channel resistance and H is the external magnetic field. Figure 2.2(e) shows magnetoresistance as a function of external magnetic field for V_{G1} = 0 and 15 V. Nonzero magnetoresistance is observed only for V_{G1} = 15 V, and increases to values as high as 80% for an external field of 5 kOe. We also fabricated a device with a uniform planar gate structure, but for reasons described below $\Delta R / R_0$ and MR were both found to be zero for this device.

The mechanism we propose as being responsible for the observed electrical behavior is illustrated schematically in Figure 2.2(f). Application of a gate voltage V_{G1} modulates strain in the $SrTiO_3$ layer through the existence of a piezoelectric response, specifically the converse piezoelectric effect in which the electric field produced by V_{G1} leads to mechanical deformation of the $SrTiO_3$. The resulting strain field extends into the adjacent $LaCoO_3$ layer, allowing the strain in that layer to be modulated by the gate voltage as well. Because a critical minimum level of tensile strain is required to induce ferromagnetism in the $LaCoO_3$ layer, [52, 54] varying V_{G1} allows strain in the $LaCoO_3$ layer to be modulated across the critical level required to induce the transition to ferromagnetic behavior, enabling electrical control of ferromagnetism in $LaCoO_3$ to be achieved. As previously reported, [54] ferromagnetism occurs in the $LaCoO_3$ layer above a threshold value of tensile strain; for lower strain values, the $LaCoO_3$ is nonmagnetic. The XRD data shown in Figure 2.1(e) suggest that the tensile strain of $LaCoO_3$ without

gate bias is in the vicinity of this critical point, so that modulation of ferromagnetism of the $LaCoO_3$ would require an in-plane strain change of order ~0.1%. The dependence of channel resistance on gate voltage and magnetic field then arises as a consequence of spatially dependent modulation of ferromagnetism in the $LaCoO_3$ channel due to the geometry of the gate contacts, and increased carrier scattering at ferromagnet-nonmagnet interfaces within the channel. It should be noted that screening of the gate electric field by the thin $LaCoO_3$ layer is weak due to the low carrier density in that layer at low temperatures (e.g. 77 K), and therefore most of the electric field under a sufficient gate bias (e.g. 15 V) still enters the $SrTiO_3$ layer beneath.

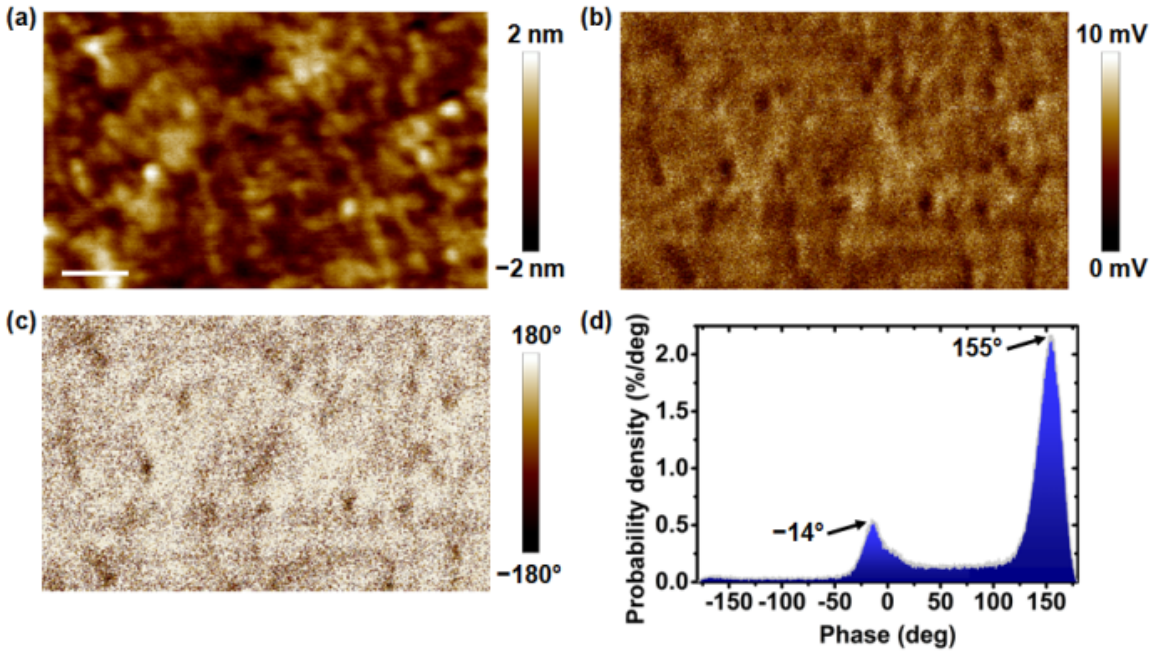


Figure 2.3: (a) Surface topography. Scale bar is 150 nm. (b) PFM lateral amplitude image. (c) PFM lateral phase image. (d) PFM lateral phase histogram. Nonzero signal in the PFM amplitude image confirms the existence of piezoelectric response in the structure, while the histogram showing a bimodal phase response distribution indicates the presence of one dominant orientation for piezoelectric response, and the existence of smaller regions with inverted orientation.

Key to this mechanism is the existence of piezoelectric response in the $SrTiO_3$ layer. Figure 2.3 shows results of PFM [74] measurements performed on a $LaCoO_3$(30 nm)/ $SrTiO_3$(8 nm) heterostructure grown on Si (001). Room-temperature piezoelectric response, which in our $SrTiO_3$ layers can be stabilized by compressive strain [60–62] imposed by the upper $LaCoO_3$ layer, is clearly visible in images of both amplitude (Figure 2.3(b)) and phase (Figure 2.3(c)), and the statistical distribution of PFM phase response shown in Figure 2.3(d) unambiguously indicates the existence of a dominant material polarity, verifying the poled nature of the piezoelectric $SrTiO_3$ layer and consistent with the observation that only a positive gate voltage (above a threshold) results in current suppression. While the PFM measurements shown here were performed at room temperature, earlier studies have indicated that piezoelectricity in $SrTiO_3$ can be maintained and, indeed, increase at low temperature. [59] Similar measurements were performed on samples in which the $SrTiO_3$ layer was replaced by MBE-grown heavily La-doped highly conductive $SrTiO_3$ in which sufficient carriers are activated from the La doping level and the electric field across the $SrTiO_3$ layer would be dramatically reduced or eliminated due to free carrier screening; no PFM response was observed, indicating that the piezoelectric response shown in Figure 2.3 arises from $SrTiO_3$ rather than $LaCoO_3$.

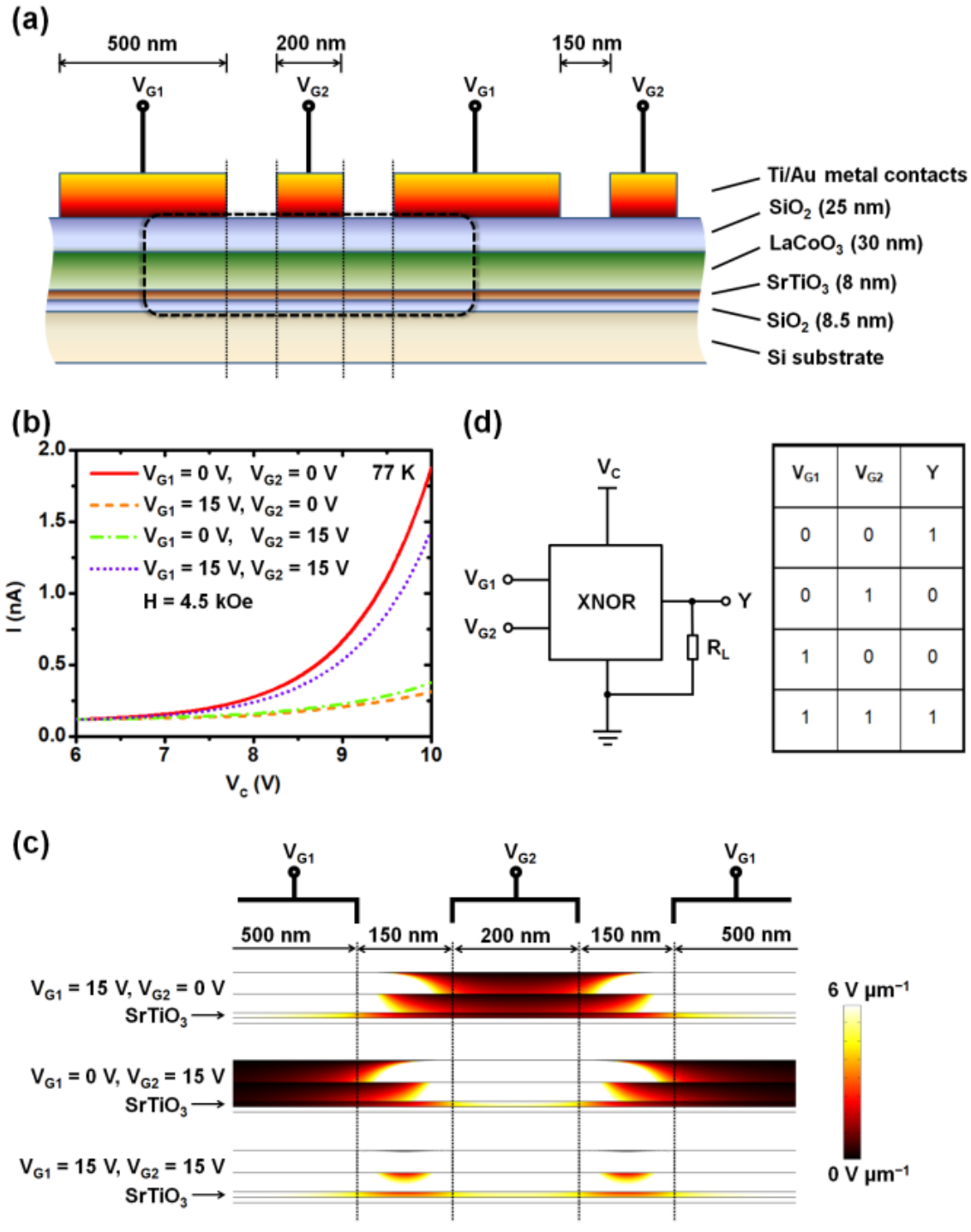

(a)
500 nm
200 nm
150 nm
V_{G1}
V_{G2}
V_{G1}
V_{G2}
Ti/Au metal contacts
SiO_2 (25 nm)
$LaCoO_3$ (30 nm)
$SrTiO_3$ (8 nm)
SiO_2 (8.5 nm)
Si substrate
(b)
V_{G1} = 0 V, V_{G2} = 0 V
77 K
V_{G1} = 15 V, V_{G2} = 0 V
V_{G1} = 0 V, V_{G2} = 15 V
V_{G1} = 15 V, V_{G2} = 15 V
H = 4.5 kOe
I (nA)
V_C (V)
(d)
V_C
V_{G1}
V_{G2}
XNOR
Y
R_L
V_{G1} V_{G2} Y
0 0 1
0 1 0
1 0 0
1 1 1
(c)
V_{G1}
V_{G2}
V_{G1}
500 nm
150 nm
200 nm
150 nm
500 nm
V_{G1} = 15 V, V_{G2} = 0 V
$SrTiO_3$
V_{G1} = 0 V, V_{G2} = 15 V
$SrTiO_3$
V_{G1} = 15 V, V_{G2} = 15 V
$SrTiO_3$
6 V μm⁻¹
0 V μm⁻¹

Figure 2.4.

Figure 2.4: (a) Cross-sectional view of device geometry and contact configuration for finite-element modeling of electric field distribution. Simulation results of the circumscribed region are shown in (c). (b) Channel current vs. V_C at 77 K with H = 4.5 kOe for (i) V_{G1} = 0 V, V_{G2} = 0 V; (ii) V_{G1} = +15 V, V_{G2} = 0 V; (iii) V_{G1} = 0 V, V_{G2} = +15 V; and (iv) V_{G1} = +15 V, V_{G2} = +15 V. Different gate biasing configurations lead to different electric field distributions and therefore variations in modulation of strain in the $SrTiO_3$ layer, and of ferromagnetism in the $LaCoO_3$ layer. (c) Finite element simulations of electric field (vertical component) distributions in the $SrTiO_3$ layer for gate voltage applied in different configurations. In the first two cases where +15 V is applied to either set of gate fingers, well-defined unbiased regions in the $SrTiO_3$ layer can be found. In the third case, fringing fields at the gate contact edges penetrate the unbiased region, leading to laterally extended modulation in electric field and consequently strain. This expansion in electric field modulation results in reduced modulation of channel current in the case of $V_{G1} = V_{G2}$ = +15 V. (d) Schematic diagram (left) and truth table (right) for a two-input exclusive-NOR (XNOR) logic gate implemented by our device structure. High (low) voltage is defined as 1 (0) for both inputs and output so that $Y = V_{G1} \odot V_{G2}$.

Investigation of the influence of gate finger geometry provides further insight into the roles of strain, strain-dependent ferromagnetism, and ferromagnet-nonmagnet interface scattering on electronic transport characteristics. Figure 2.4(a) shows a cross-sectional schematic of the device geometry illustrated in Figure 2.1, with two sets of interdigitated gate fingers of length (in the direction of channel current transport) 500 nm and 200 nm separated by gaps of 150 nm between adjacent fingers, to which voltages V_{G1} and V_{G2}, respectively, are applied. Figure 2.4(b) shows channel current, measured at 77 K with H = 4.5 kOe, as a function of V_C for different gate voltage configurations. High channel current is observed for $V_{G1} = V_{G2} = 0$ V, while much lower current is observed when +15 V is applied to one, but not both, sets of gate fingers – consistent with the influence of ferromagnet-nonmagnet interface scattering that arises when regions of nonmagnetic material are created by application of positive voltage to one set of gate fingers. However, high current flow is observed for $V_{G1} = V_{G2} = +15$ V.

The origin of this ostensibly counterintuitive observation is revealed in Figure 2.4(c), which shows a finite-element numerical simulation of the vertical component of electric field within the device region indicated by the dashed line in Figure 2.4(a) for different gate voltage configurations. Note that the simulated vertical electric field in the $SrTiO_3$ layer is approximate since the dielectric constant used for $SrTiO_3$ in the simulation is assumed to be $300\varepsilon_0$, which is for strain-free $SrTiO_3$ at room temperature and not necessarily applicable to piezoelectric strained $SrTiO_3$ thin films. [62] Nevertheless, the electric field distribution profile elucidated by the simulation is qualitatively correct, and sufficient to illustrate the key points in our discussion. For $V_{G1} = V_{G2} = 0$ V (not shown), no electric field, and consequently no strain modulation arising from the converse piezoelectric effect, is present. When either V_{G1} or V_{G2} (but not both) is increased to +15 V, there is a strong modulation of the electric field, and consequently

strain, along the length of the channel, resulting in alternating regions of ferromagnetic and nonmagnetic $LaCoO_3$ in the channel. The resulting interface scattering leads to reduced channel current, as seen experimentally in Figure 2.4(b). For $V_{G1} = V_{G2} = +15$ V, however, the spacing between adjacent gate fingers is sufficiently small that the fringing fields at the edge of each gate finger yield much weaker variation in electric field, and consequently strain, along the length of the channel. As a result, the transition from ferromagnetic to nonmagnetic behavior occurs throughout the channel, resulting in high channel current due to the absence of interfacial scattering except at the ends of the channel region. We also note that this behavior further excludes the conventional MOSFET working mechanism as being responsible for the observed effect and, more interestingly, allows the device to provide exclusive-NOR logic functionality, as illustrated in Figure 2.4(d).

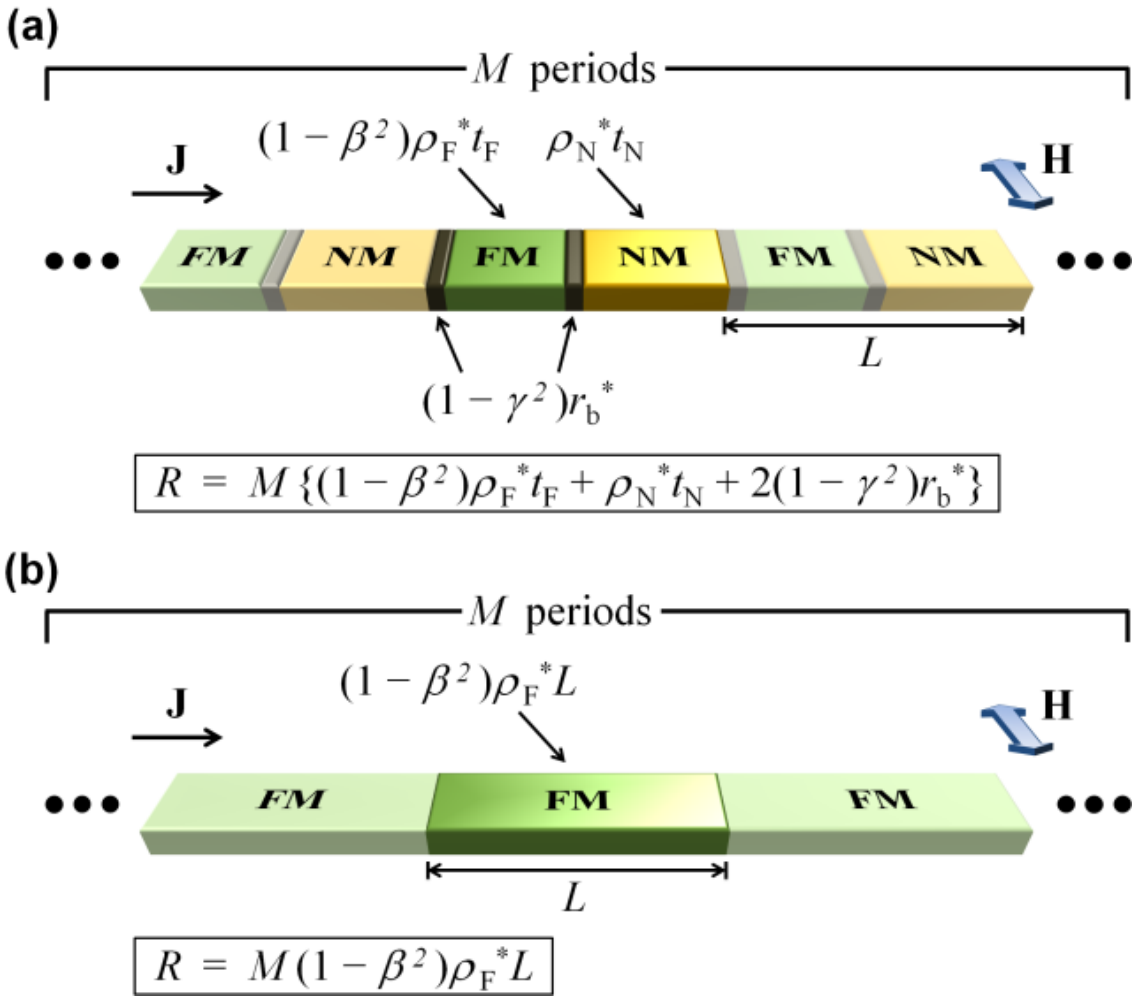


Figure 2.5: (a) The Valet-Fert current channel model for the case of $V_G > V_{th}$. β and γ are bulk spin polarization in ferromagnetic $LaCoO_3$ and interfacial spin polarization at the interface between ferromagnetic $LaCoO_3$ and nonmagnetic $LaCoO_3$, respectively. Both ρ_F^* and ρ_N^* are resistivity of the $LaCoO_3$ channel at 77 K, L is the length of the channel for one period within which t_F (t_N) is length of the ferromagnetic (nonmagnetic) channel, and M is the total number of periods in the channel. Nonmagnetic regions form and lead to nonzero magnetic domain wall resistances at the interface with ferromagnetic regions so that three terms, i.e., $(1-\beta^2)\rho_F^* t_F$ from ferromagnetic $LaCoO_3$, $\rho_N^* t_N$ from nonmagnetic $LaCoO_3$, and $2(1-\gamma^2)r_b^*$ from magnetic domain walls, contribute to the total channel resistance R. (b) The Valet-Fert model for $V_G < V_{th}$. The entire channel is ferromagnetic and domain wall resistance is absent, in which case only one term $(1-\beta^2)\rho_F^* L$ contributes to R.

An analysis based on the Valet-Fert model [63] for current transport in magnetic and nonmagnetic multilayers provides both insight into factors dominating current transport in these devices, and quantitative estimates of spin polarization in the $LaCoO_3$ layer. Applicability of the Valet-Fert model to describe electrical transport in the $LaCoO_3$ film at 77 K can be confirmed from the conductivity data shown in Figure 2.1(c). As discussed above, the small-polaron transport in the $LaCoO_3$ film at temperatures below 150 K is Bloch-type band motion, analogous to carrier transport in conventional semiconductors with a large effective mass, to which the Boltzmann transport equation is applicable. [71] Valet and Fert [63] derived macroscopic transport equations, i.e., the Valet-Fert model, starting from the Boltzmann equation and formally justified its validity in the limit that the spin-diffusion length of each material is long compared to the mean free path of the same material, regardless of the layer thicknesses. This approach was further proved to be accurate for spin-diffusion lengths comparable to the mean free paths both theoretically by numerical studies of the Boltzmann equation [75] and experimentally [76]. In our device structure, the minimum length of each ferromagnetic or nonmagnetic region is 200 nm, which is expected to be much larger than the mean free path in the $LaCoO_3$ layer given the large effective mass and consequently low mobility in the small-polaron narrow band. Therefore, the Valet-Fert model can be safely used to describe electrical transport in the $LaCoO_3$ layer at low temperatures (77 K – 150 K).

Figure 2.5 shows schematic illustrations of the primary factors contributing to the resistance of the $LaCoO_3$ channel in the presence (Figure 2.5(a)) and absence (Figure 2.5(b)) of nonmagnetic regions within the ferromagnetic $LaCoO_3$. In Figure 2.5(a), alternating ferromagnetic and nonmagnetic regions of length t_F and t_N, respectively, have areal resistance $(1 - \beta^2)\rho_F^* t_F$ and $\rho_N^* t_N$, where β is the spin polarization in the ferromagnetic $LaCoO_3$ layer, and ρ_F^* and ρ_N^* are the resistivity of the ferromagnetic and

nonmagnetic segments. These segments are separated by interfacial regions of areal resistance $(1 - \gamma^2)r_b^*$, where γ is the spin polarization at the interface and r_b^* the interfacial resistance. In Figure 2.5(b), the entire channel is ferromagnetic and the resistance of a single period L is given by $(1 - \beta^2)\rho_F^* L$. To estimate the spin polarization β in $LaCoO_3$, we note that the resistance change $\Delta R / R_0$ and magnetoresistance MR, defined in equations (2.1) and (2.2), respectively, can be related to each other according to the expression

$$MR = (1 - \beta^2)\,\Delta R/R_0 - \beta^2 \quad . \tag{2.3}$$

Using values for MR and $\Delta R / R_0$ from Figure 2.2 for H = 4.5 kOe, V_C = 8 V, and V_{G1} = 15 V at 77 K, we obtain $\beta = 0.24 \pm 0.02$. An independent estimate of β can be obtained from a comparison of values for $\Delta R / R_0$ obtained using different gate dimensions, as in Figure 2.4(b). This approach yields $\beta = 0.29 \pm 0.01$, in very good agreement with that obtained from equation (2.3). Equation (2.3) also implies that MR should be independent of the number of periods, M, of the interdigitated finger structure, and therefore of the number of ferromagnet-nonmagnet interfaces traversed. It should be noted that since a magnetic field of 5 kOe is not sufficient to saturate the magnetization of our $LaCoO_3$ film, [52] the spin polarization β extracted at 5 kOe is not the spin polarization of a magnetically-saturated $LaCoO_3$ layer. The extracted spin polarization in this work, however, is still useful in validating our use of the Valet-Fert model, and more importantly, the method described to extract the spin polarization should be applicable in magnetically saturated films as well.

Table 2.1 shows measured values of MR for device structures with different gate dimensions and number of periods M, along with MR values predicted by equation (2.3) using values of $\Delta R / R_0$ measured using the same devices and spin polarization $\beta = 0.27 \pm 0.03$. As predicted, MR is seen to be independent of M, and to vary as

expected with ΔR / R_0 for different gate dimensions. The value of β obtained above together with the fact that no distinguishable resistance change was observed by applying a positive voltage to a planar gate uniformly over the entire channel further indicates that the magnetic domain wall scattering at ferromagnetic-nonmagnetic interfaces rather than the difference in conductivity of the ferromagnetic and nonmagnetic phase predominantly leads to the large $\Delta R/R_0$ and MR.

M	9		18
V_{G1} (V)	15	0	15
V_{G2} (V)	0	15	0
MR_{meas} (%)	75.0 ± 0.5	71.0 ± 0.8	75.7 ± 0.6
MR_{cal} (%)	71.8 ± 3.0	68.7 ± 3.0	72.3 ± 3.1

Table 2.1: Measured and calculated MR at V_C = 8 V, T = 77 K and H = 4.5 kOe for different gate biasing configurations and number of periods in a single device. Excellent consistency between measured MR data and corresponding values calculated using the Valet-Fert model, particularly the fact that MR is independent of M, strongly supports the basic applicability of the Valet-Fert model and the role of ferromagnet-nonmagnet interface scattering in the experimental observation.

2.4 SUMMARY

In summary, we have designed, characterized, and analyzed devices based on $LaCoO_3/SrTiO_3$ heterostructures grown on Si (001) substrates by MBE in which the combination of strain-dependent ferromagnetism in $LaCoO_3$, the converse piezoelectric effect in $SrTiO_3$, and strain coupling between these layers enables electrically controlled ferromagnetism and magnetoresistance to be achieved. Detailed mechanisms explaining this behavior are developed and verified using (i) the Valet-Fert model to quantify $LaCoO_3$ spin polarization, magnetic interfacial resistances, and the dependence of

magnetoresistance on device geometry; (ii) finite-element modeling of electric field distributions to explain variations in current transport for different gate finger geometries; and (iii) PFM studies to confirm the presence of piezoelectric response in $SrTiO_3$ films within our device structures. These results illustrate a new approach for electrically controlling local ferromagnetism in complex oxide heterostructures and for probing and controlling spin transport behavior in complex oxides at submicron dimensions, and offer the possibility of straightforward integration with conventional Si-based electronics via epitaxial growth directly on Si substrates.

Chapter 3: Resistive Switching of Single-Crystal Anatase-TiO_2 on Silicon[2]

3.1 INTRODUCTION

In recent years there has been intense interest in developing non-charge-based nanoscale nonvolatile memory (NVM) bit cells as an alternative to the current mainstream charge-based approaches as represented by flash memories, which suffer from long writing times and face tremendous challenges as transistor sizes decrease further into the nanoscale regime [77]. Among the emerging NVM technologies, metal-oxide resistive random access memory (RRAM) has received particular interest owing to its high density, excellent scalability, simple device structures, low power consumption, fast switching speed, and compatibility with conventional complementary metal-oxide-semiconductor (CMOS) technology [78–80].

TiO_2 is one of the most extensively studied metal oxides that exhibit resistive switching behavior, and has enjoyed particular prominence for RRAM applications, memristors, reconfigurable analog integrated circuits, stateful implication logic, and neuromorphic computing [81–95]. In addition, TiO_2 is particularly intriguing in that both unipolar resistive switching (URS) and BRS have been reported [91], enabling it to serve as a rich platform for studying and comparing different RS mechanisms concurrently [79, 81], including thermochemical [88, 89], valence change [84], and electrostatic/electronic switching [90, 93]. Regardless of the specific RS behavior that TiO_2 demonstrates,

---

[2] Part of the content of Chapter 3 has been published as C. Hu, M. D. McDaniel, J. G. Ekerdt, and E. T. Yu, "High ON/OFF ratio and quantized conductance in resistive switching of TiO_2 on silicon", *IEEE Electron Device Lett*. **34**, 1385—1387 (2013), and as C. Hu, M. D. McDaniel, A. Posadas, A. A. Demkov, J. G. Ekerdt, and E. T. Yu, "Highly controllable and stable quantized conductance and resistive switching mechanism in single-crystal TiO_2 resistive memory on silicon", *Nano Lett*. **14**, 4360—4367 (2014). C. Hu designed, modeled, fabricated, characterized, and analyzed the devices involved in this work. M. D. McDaniel and J. G. Ekerdt contributed to the growth and X-ray photoelectron spectroscopy studies of the epitaxial TiO_2 thin films. E. T. Yu supervised the work in every aspect. All the authors contributed to the writing and revision of the manuscripts.

oxygen vacancies are always believed to play a critical role in the RS of TiO_2, as indicated both theoretically [96, 97] and experimentally [82, 83, 95, 98, 99].

By far almost all work on RS in metal oxides has been on polycrystalline or amorphous oxides. In this work, RS of single-crystal anatase TiO_2 grown epitaxially on Si (001) is investigated in detail, and shown to originate from a valence change mechanism rather than thermochemical or electrostatic/electronic switching, but to behave electrically in a manner very similar to electrochemical metallization memory, and quite different from typical polycrystalline or amorphous TiO_2 RS elements [81–85, 88–95, 98, 99]. Key characteristics of the RS we observe in single-crystal anatase TiO_2 include a record high ON/OFF ratio (10^6–10^7), small electronic leakage current in the HRS [100], low RESET current, and highly controllable and reproducible QC in the low-resistance state (LRS). The demonstrated resistive switching behavior is fundamentally different as compared to what has been observed in more conventional structures to date.

For many RRAMs, the formation and rupture of nanoscale conductive filaments (CF) within an insulating matrix is widely accepted as the major working mechanism [78, 79]. In fact, the prediction that ideally a CF can be shrunk to the atomic scale has helped to trigger extensive research efforts in the RRAM field. Quantized conductance [101] for the low-resistance state of RS is an inevitable consequence of scaling of filamentary-type RRAM cells to nanoscale dimensions, and has been suggested to be of potential interest for building synaptic devices [102–104]. For these reasons, combined with their compatibility with silicon-based CMOS technology, binary oxides have been a subject of intense research interest in recent years for demonstration and investigation of quantized conductance phenomena. Previous reports have shown that conductance quantization can occur in metal oxides or silicon oxide without using Ag or Cu as an active electrode [105–110]. However, these results are either associated with transient current jumps (i.e.,

conductance changes) during the SET/RESET process that significantly limit the usefulness of the observed QC, or obtained from dc resistance recorded at a specific voltage in a nonlinear LRS current-voltage (*I–V*) characteristic, leading to ambiguity when interpreting the measured resistance. More importantly, effective control over stabilized QC of a nanofilament by electrical means is generally absent. Here, highly stable QC is unambiguously demonstrated in epitaxial single-crystal anatase TiO_2 RRAM cells, with the number of quantized channels reproducibly controlled by the compliance current applied during the SET process. This behavior enables epitaxial TiO_2 RS devices to offer the possibility of working as a practical multilevel cell and as a platform for exploring novel electrical properties associated with metallic nanophases present in metal oxides. A physics-based analytical model for the SET and RESET processes is developed to account for our experimental findings that are fundamentally different from those previously reported in other literature.

3.2 Experimental Details

Epitaxial single-crystal anatase TiO_2 thin films of 8 nm thickness were grown by ALD on n+ Si (001) substrates ($\rho \sim 0.01\ \Omega\cdot$cm) with a thin single-crystal strontium titanate (STO) buffer layer. The four unit cells of STO grown by MBE serve as a template for ALD growth. The TiO_2 film is crystalline as-deposited on STO-buffered Si (001) with no post-deposition annealing required.

The TiO_2 films were analyzed by *in situ* X-ray photoelectron spectroscopy (XPS). For the 8 nm TiO_2 film, XPS spectra were taken before and after ALD growth. XPS is performed with a VG Scienta R3000 electron analyzer with a monochromated Al Kα x-ray source. The analyzer is calibrated using a silver foil, where the Ag $3d_{5/2}$ core level is defined to be 368.28 eV. High-resolution spectra of the Ti 2*p*, O 1*s*, and Si 2*p* peaks are

measured using a pass energy of 100 eV with an analyzer slit width of 0.4 mm. Each high-resolution scan is measured four times and summed, using 50 meV steps with a dwell time 157 ms per step. Film composition was determined using CasaXPS (ver. 2.3.16) peak fitting with a Shirley background subtraction.

200 μm diameter circular top electrode contacts to the TiO_2 were formed by photolithography, e-beam evaporation of 5 nm Ti/ 160 nm Au, and lift-off. Metallic Ti overlayers deposited on TiO_2 (both bulk crystal and thin film) have been shown to produce a region of interfacial suboxide, TiO_x ($x < 2$). This interfacial layer is present even when Ti is deposited at a low temperature and is reported to be ~2 nm thick [111, 112]. Therefore, a non-stoichiometric TiO_x interlayer is expected at the top Ti/TiO_2 interface due to oxygen gettering by the metallic Ti overlayer [84]. The back surface of the n+ Si substrate was coated with 8 nm Ti/ 100 nm Au as a bottom electrode. The RS behavior of the films was measured in air at room temperature by an Agilent 4156A precision semiconductor parameter analyzer in *I–V* sweep mode. The sweeping voltage *V* was applied to the top electrode with the bottom electrode grounded. The compliance current I_{comp} was fixed at 100 μA for electroforming, whereas during the SET process, I_{comp} was set between 10 μA and 1 mA to prevent hard breakdown in the TiO_2 films. The HRS and LRS resistances (R_{HRS} and R_{LRS}) were measured at a read voltage of +0.1 V.

3.3 Results and Discussion

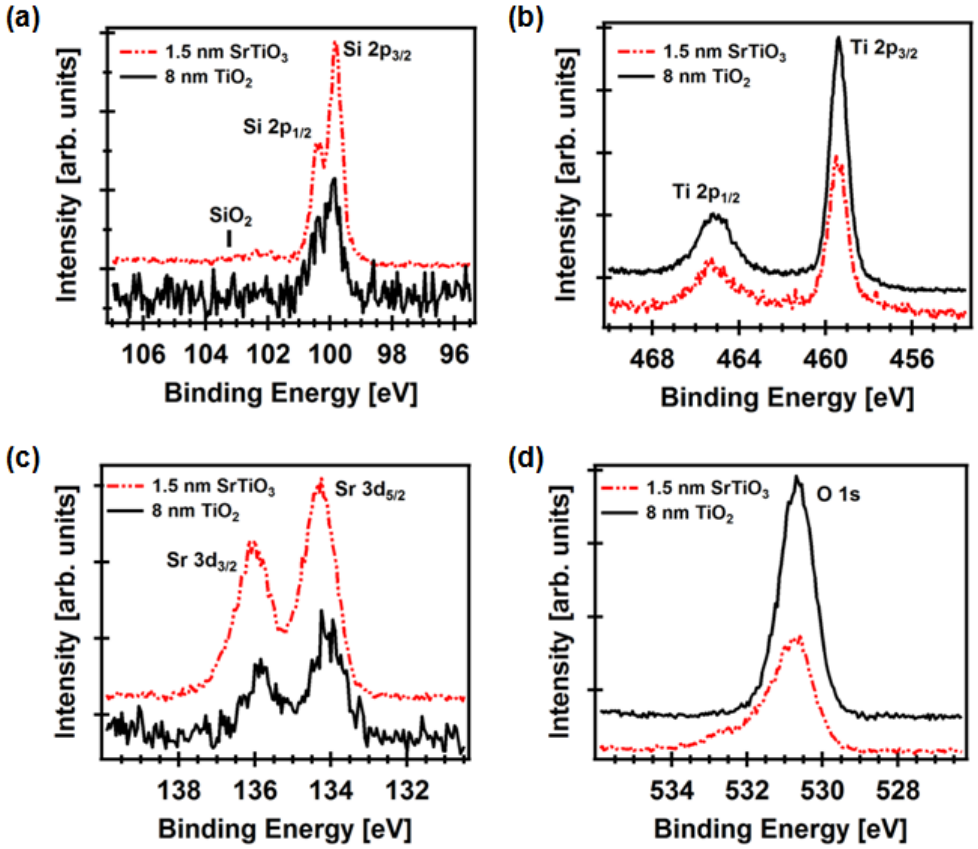


Figure 3.1: X-ray photoelectron spectra taken of a four-unit-cell (1.5 nm) $SrTiO_3$ buffer layer on Si (001) (dashed red line) and after 8-nm-thick epitaxial TiO_2 grown by ALD (solid black line). The high resolution core-level scans are shown for (a) Si 2*p*, (b) Ti 2*p*, (c) Sr 3*d*, and (d) O 1*s*.

Stoichiometric TiO_2 films were deposited on STO-buffered Si (001). High resolution core-level spectra of the Si 2*p*, Ti 2*p*, Sr 3*d*, and O 1*s* were taken before and after TiO_2 film growth on the single-crystal STO buffer layer on Si, as shown in Figure 3.1. The Ti $2p_{3/2}$ peak is located at 459.4 eV for the 8 nm TiO_2 film, indicating that the Ti is fully oxidized. We note, however, that the sensitivity of XPS is not sufficient to detect oxygen deficiencies of much less than 1%, which can lead to significant changes in the electrical conductivity. While the presence of a low concentration of oxygen vacancies

within the as-grown TiO_2 cannot, therefore, be excluded on the basis of XPS, electrical measurements indicate that the as-grown TiO_2 film is highly resistive. The Si 2*p* spectrum confirms that there is negligible SiO_2 formation after MBE growth of the single-crystal STO buffer layer. A small presence of silicon suboxide (SiO_x) is observed at ~102.2 eV, although the thickness of this layer is estimated to be 5 Å or less [113].

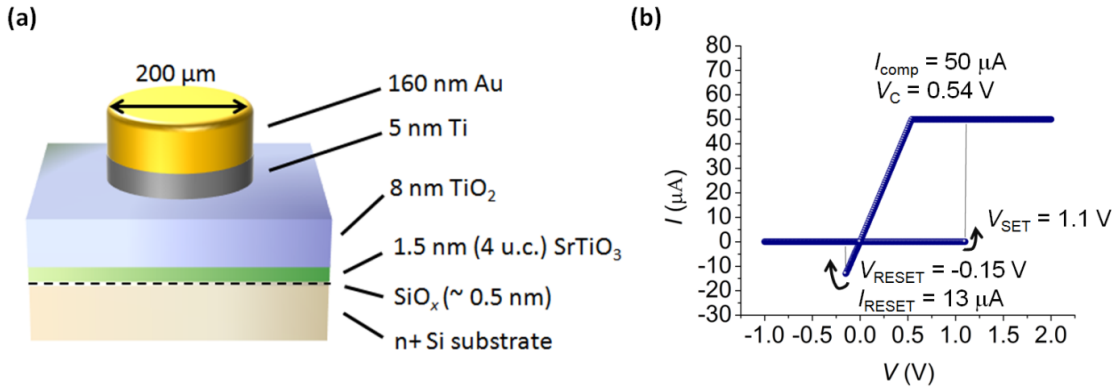


Figure 3.2: (a) Device structure for single-crystal TiO_2 cells; (b) typical *I–V* characteristics.

The device structure for the epitaxial TiO_2 RS cells is shown schematically in Figure 3.2(a). The typical RS *I–V* characteristics of such a device, shown in Figure 3.2(b), exhibit linear *I–V* behavior in the LRS and abrupt, clean RS for both SET and RESET processes. A detailed analysis of the electrical behavior provides important insights into the specific RS mechanism involved in this material system. There are five basic mechanisms that are used to explain redox-based RS in various materials [79] – the electrostatic/electronic mechanism, the valence change mechanism, the thermochemical mechanism [114–116], the electrochemical metallization mechanism [117], and the phase change mechanism [118]. For transition metal oxides such as TiO_2, the phase change mechanism, i.e., temperature-induced transition between amorphous and crystalline phases, can be eliminated at the outset as the RS mechanism [118]. Detailed analysis of

HRS *I–V* characteristics, as described below, allows all but one of the other mechanisms to be eliminated as well.

The electrostatic/electronic mechanism has been reported as a BRS mechanism in polycrystalline and amorphous TiO_2. In these materials, SET (RESET) occurs due to trapping (detrapping) of electrons in the switching layer (i.e., the layer adjacent to the top contact), which contains a high density of electron traps (typically oxygen vacancies), by applying a negative (positive) voltage to the top contact [90, 93]. For the single crystal anatase TiO_2 films in our work, the oxygen-deficient layer lies at the top of the structure, and therefore the bias voltage polarities for which the SET and RESET processes occur are contrary to those expected for the electrostatic/electronic mechanism. In addition, for RS devices that operate based on the electrostatic/electronic mechanism, space-charge-limited-current conduction governs electrical transport and leads to nonlinear (square-law) *I–V* characteristics in the LRS, the ON/OFF ratio is usually small [90, 93], and there should be no sudden transition from the LRS to the HRS during RESET, all of which are contrary to the behavior found in this work. Thus, we conclude that the electrostatic/electronic-based mechanism is not responsible for the BRS of the single-crystal anatase TiO_2 films studied here.

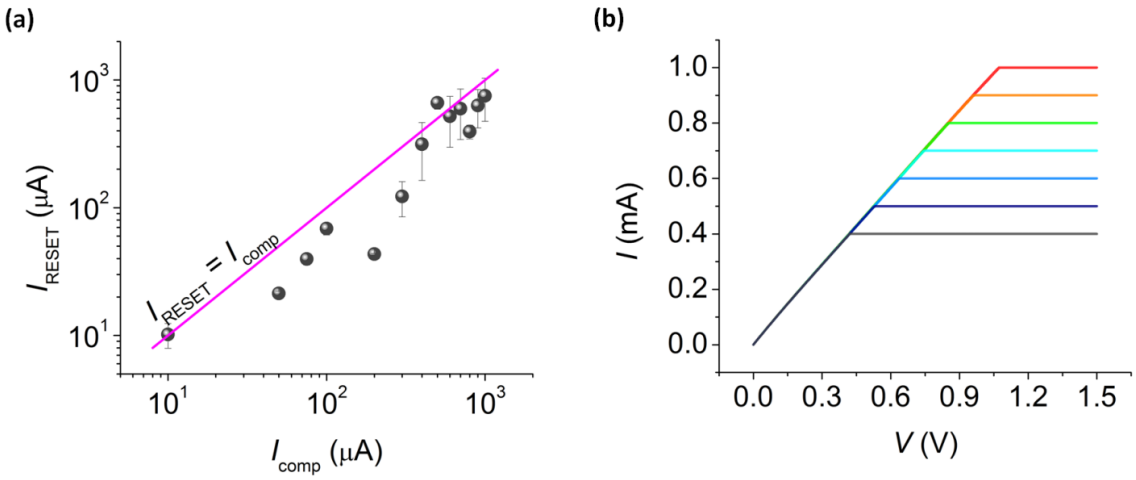


Figure 3.3: Electrical characteristics for the single-crystal TiO_2 device which contradict with those of thermochemical or heat-induced RS mechanism. (a) I_{RESET} vs. I_{comp} for I_{comp} ranging from 10 μA to 1 mA; (b) *I–V* characteristics of a set of dc double sweeps, each starting from $V = 0$ V but with an incremental I_{comp} (from 400 μA to 1 mA), after the SET process under $I_{comp} = 400$ μA.

RS via the thermochemical mechanism relies on rupture of CFs by self-accelerated diffusion of oxygen vacancies due to Joule heating and is responsible mainly for URS as well as BRS in some metal oxides [114–116]. In the case of thermochemical-based URS and BRS, the peak value of electric current during RESET, I_{reset}, is found empirically to be proportional to the compliance current, I_{comp}, with a universal ratio I_{reset} / I_{comp} of about 1.2, irrespective of the URS/BRS mode and of the metal oxide material used in the RRAM device [114–116]. For the TiO_2 devices in this work, however, I_{reset} is smaller than I_{comp} over a wide range of I_{comp}, as shown in Figure 3.3(a), and the power dissipation at which RESET occurs is therefore smaller than the power dissipated by the device in the ON state following the SET process for nearly all the different I_{comp} values tested. Figure 3.3(b) shows the *I–V* characteristics of a set of dc double sweeps (i.e., an upsweep followed by a downsweep), each starting from $V = 0$ V but with I_{comp} increasing in 0.1 mA steps. The first sweep is with $I_{comp} = 0.4$ mA, right after the SET process under

the same I_{comp}. It can be seen that for the following sweeps with I_{comp} incrementally increasing, R_{LRS} is always very stable and maintains the same value as that for the first sweep with I_{comp} = 0.4 mA. Even with I_{comp} for the last sweep at 1.0 mA, which is much larger than the corresponding I_{reset} ~ 0.38 mA during the follow-up negative voltage sweep (not shown), R_{LRS} remains at the same value, indicating that the CF formed in the SET process is highly stable against either growth or rupture. Positive voltage sweeps with I_{comp} = 10 mA and the same voltage peak value and sweep rate as for the former SET process (for which I_{comp} = 10 μA–1 mA) were also performed (not shown); no URS behavior was observed under this condition. This observation together with Figures 3.3(a) and (b) unambiguously excludes the possibility of interpreting the RESET process as mainly being the result of heat-induced rupturing of the CF. It should be noted, however, that Joule heating could still play a minor role for the RESET processes in this material system, and thermochemical-based URS could potentially be achieved in our system by applying a voltage sweep with I_{comp} much larger than 10 mA.

The high ON/OFF ratio, low electronic leakage in the HRS, and linear *I–V* characteristics in the LRS found for the single-crystal anatase TiO_2 devices are highly reminiscent of features typically observed in electrochemical-metallization based systems [79, 102–104], in which a CF consisting of metal atoms with high ionic mobility (typically Ag or Cu) bridges the whole film during SET and mostly dissolves during RESET. However, in our material system, Ti/Au is used as the top metal contact and titanium is not a highly mobile ionic species – in fact, positively charged oxygen vacancies are even more mobile than titanium ions [78, 79] and are considered as the major mobile species driving the RS behavior in TiO_2 [79, 82, 83, 96–99]. Therefore, the only remaining possible mechanism that could be responsible for the RS observed in our material system is the valence change mechanism. Although this conclusion is consistent

with previous reports on TiO_2 RRAM cells [79, 84], the electrical characteristics of single-crystal anatase TiO_2 RS devices are very different from, and generally superior to, those typically observed for amorphous or polycrystalline TiO_2.

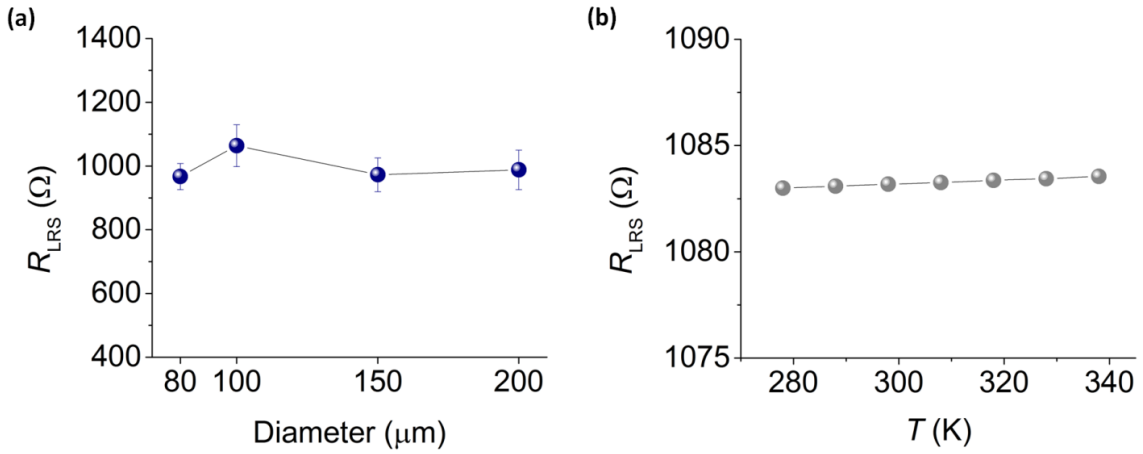


Figure 3.4: (a) R_{LRS} vs. device size (in diameter) after SET processes (30 SET processes for each device size) under I_{comp} = 500 μA, showing no dependence of R_{LRS} on the device electrode area; (b) R_{LRS} vs. T for a particular ON-state of the 200 μm diameter device after SET under I_{comp} = 500 μA, demonstrating a metallic conduction behavior in the LRS.

Valence change-based BRS typically occurs in transition metal oxides with electrodes that do not inject metal cations due to the fact that the electrode metal is not easily oxidized (e.g., Pt or Au) or that the oxidized form is not easily reduced back to the metal (e.g., Al, Ti or Nb). This type of RS normally involves a localized (laterally for filamentary RS and vertically for interfacial area distributed RS) enrichment or depletion of oxygen vacancies by applying bias voltages of opposite polarities [79]. Interfacial RS based on the valence change mechanism relies on the modulation of a Schottky barrier by movement of an ionic species into or out of that barrier layer [84], which typically shows electrode area-dependent R_{LRS}. In this respect, RS based on height and/or width modulation of a Schottky barrier is inconsistent with the linear LRS *I–V* characteristics

and abrupt transitions from the HRS to the LRS during RESET observed for our material system [79, 84]. Figure 3.4(a) compares R_{LRS} (after SET at I_{comp} = 500 μA) for top electrodes of different sizes (80 μm, 100 μm, 150 μm, and 200 μm in diameter, respectively), where R_{LRS} is found to be almost constant over different device sizes, suggesting the filamentary nature of the LRS. Shown in Figure 3.4(b) is R_{LRS} as a function of temperature (278–338 K) around room temperature for a particular ON-state of the 200 μm device after SET at I_{comp} = 500 μA. R_{LRS} is clearly seen to be essentially constant, increasing by less than 1 Ω when the temperature increases from 278 K to 338 K, indicating that ballistic conduction across a nanoscale channel, with minimal additional series resistance, occurs. Therefore, we conclude that the filamentary-type valence change switching mechanism applies to the RS of our materials stack, i.e., Au/Ti/single-crystal anatase TiO_2/STO/n+ Si.

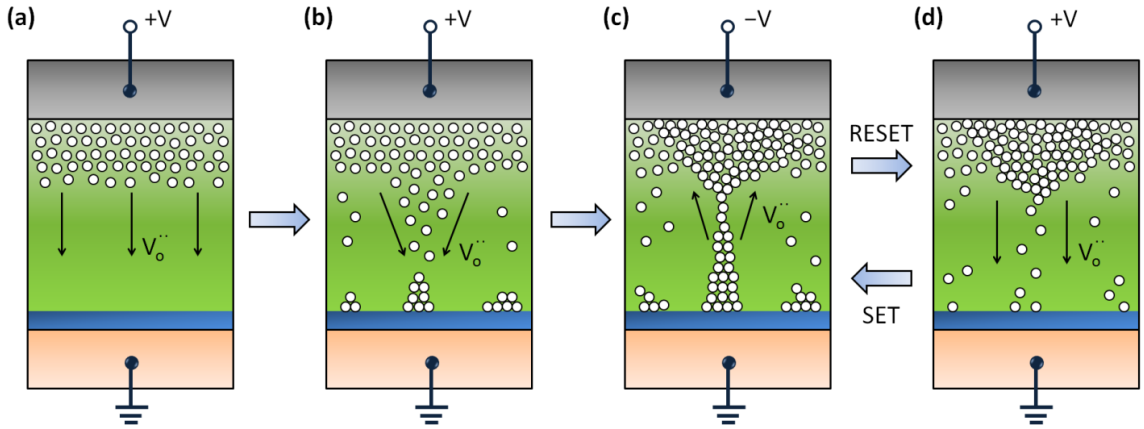


Figure 3.5: Illustration of the proposed RS mechanism based on the *I–V* characteristics. In each part of the illustration, voltage is applied to the top contact after the depicted oxygen vacancy configuration is achieved within the TiO_2 matrix, and the arrows denote moving direction of oxygen vacancies upon application of voltage to the top contact. Oxygen vacancy configuration (a) in the pristine state, (b) during the SET process, (c) in the ON state, and (d) in the OFF state.

The filamentary-type valence change based switching mechanism for the single-crystal TiO_2 device is therefore proposed to be as follows. In an as-fabricated TiO_2 device, an oxygen-deficient layer is only present at the top of the TiO_2 layer due to the top Ti metallization [84], as shown in Figure 3.5(a). We have determined experimentally that a single-crystal TiO_2 device is not switchable with a pure Au top electrode (specifically, for an 80 s double sweep of voltage with a peak voltage of +5 V). This behavior is different from that of conventional valence change memories, in which oxygen vacancies can easily be generated at the interface with a noble-metal anode during electroforming and the resulting ON/OFF ratio is usually small [79]. This indicates that for a top electrode made of noble metal in contact with the single-crystal anatase TiO_2 film, the number of oxygen vacancies electrochemically generated during the electroforming/SET process (within the typical timescale employed in this work) is insufficient to form extended defects as the seed for a filamentary switching event [79]. In contrast, a top oxygen-deficient layer, serving as a reservoir of oxygen vacancies, helps to achieve a very high ON/OFF ratio without causing hard breakdown of the RS active layer.

By applying a positive bias voltage to the top contact, oxygen vacancies drifting from the top oxygen-deficient layer are partially reduced and re-deposited upward from the bottom, i.e., the TiO_2/STO interface (Figure 3.5(b)) [97], This process leads to localized formation of a CF, assisted by local roughness of the oxygen vacancy cluster distribution at the bottom that enables CF nucleation at a local asperity, to complete the SET process (Figure 3.5(c)). Since Ti_nO_{2n-1} (n = 3–5 for rutile and 5–7 for anatase) Magnéli or Magnéli-like nanophases are the only known structural configurations of oxygen vacancies in TiO_2 that demonstrate metallic and resistively switchable behaviors [95, 98, 99, 119], and the LRS I–V behavior observed in this work is metallic (Figure

3.4(b)), we postulate that the CF formation in the anatase TiO_2 is attributable to an energetically-favorable local phase transformation to a Magnéli-like nanophase by one-dimensional (laterally confined) nucleation of extended defects composed of migrating oxygen vacancies at a random site(s) for each SET process [78, 79, 95, 98]. In addition, SET could also occur in the STO and/or SiO_x layers since the observed LRS *I–V* characteristics are highly linear indicating the absence of a 2 nm thick STO/SiO_x tunnel barrier.

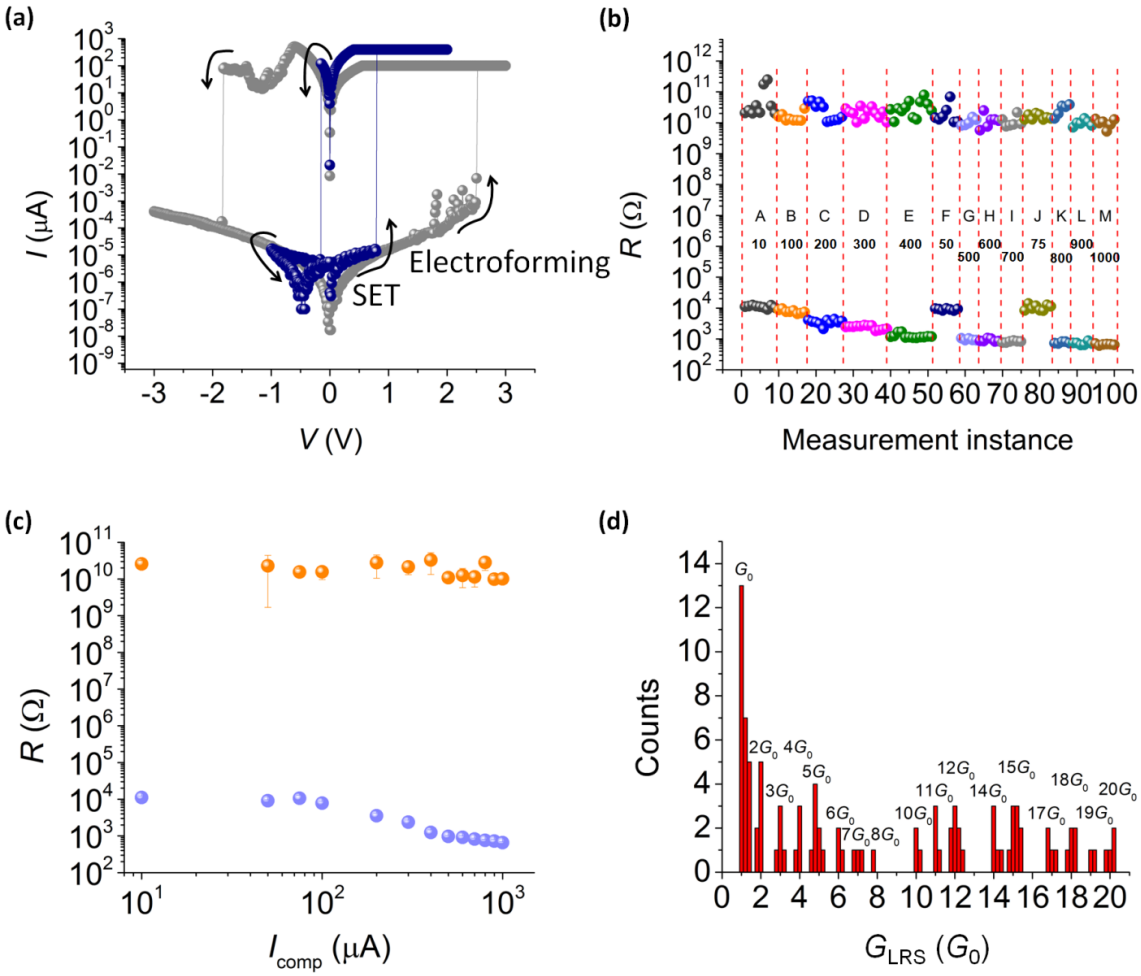


Figure 3.6.

Figure 3.6: Electrical performance of an 8 nm thick single-crystal TiO_2 device. (a) Log *I–V* of typical RS characteristics of an electroforming sweep (grey) and a regular RS sweep (blue); (b) R_{HRS} and R_{LRS} over 100 successive switching sweeps, with letters A to M indicating different I_{comp} applied during SET process of those sweeps (A – 10 μA, B – 100 μA, C – 200 μA, D – 300 μA, E – 400 μA, F – 50 μA, G – 500 μA, H – 600 μA, I – 700 μA, J – 75 μA, K – 800 μA, L – 900 μA, M – 1 mA); (c) R_{HRS} and R_{LRS} vs. I_{comp} based on the data shown in (b), where saturation of the R_{LRS} increase at smaller I_{comp} can be seen; (d) Histogram of G_{LRS} in units of $G_0 = 2e^2/h$ for the 100 successive cycles shown in (b), in which distribution of discrete peaks around integers of G_0 is clearly seen.

During the RESET process, the CF dissolves owing to the electrochemical current through the TiO_2 matrix, followed by the electric-field driven oxygen vacancy drift back to the top, as shown in Figure 3.5(d). Figure 3.6(a) shows that the pristine-state current (i.e., OFF-state current before electroforming) is the same order of magnitude as the subsequent OFF-state current. This indicates that during the last stage of the RESET process [immediately after reaching the RESET voltage, −0.15 V in this case, cf. Figures 3.2(b) and 3.6(a)], most of the dissolved positively-charged oxygen vacancies are driven by the large electric field back toward the top electrode, leaving the single-crystal anatase TiO_2 layer beneath with very few oxygen vacancies. On the other hand, the electroforming threshold voltage is higher than the SET voltage, as shown for example in Figure 3.6(a) and also observed for a wide range of SET compliance currents, indicating that during electroforming, additional oxygen vacancies are created by movement of oxygen atoms from the Ti/TiO_2 interface into the Ti electrode [84], lowering the threshold voltage for the subsequent SET processes. We also note that in Figure 3.6(a), the *I–V* curve after RESET in the regular SET/RESET cycle does not go through the origin, which may indicate the emergence of the recently reported nanobattery effect for redox-based RS systems [120].

Figure 3.6(b) shows R_{HRS} and R_{LRS} measured over 100 dc sweep cycles under I_{comp} ranging from 10 μA to 1 mA. Here, each R_{LRS} was measured right after a SET process under the corresponding I_{comp}, which is different from the measurement scenario for Figure 3.3(b). Very high ON/OFF ratios of 10^6–10^7 are observed over the entire range of I_{comp}. This is unusual for filamentary-type valence change memory with a top electrode in the size range employed here (200 μm in diameter), for which the ON/OFF ratio is generally small due to the fact that filamentary RS only affects a tiny portion of the entire electrode area and the remaining electrode area normally contributes to a non-switching

parallel resistance by means of electron tunneling or hopping through point defects (e.g., oxygen vacancies and/or reduced metal ions) within the insulating oxide matrix [79]. In this respect, the single-crystal nature of the TiO_2 could play a key role, with high crystallinity and film quality helping to minimize the intrinsic defects, and greatly suppress the background electric current in both states of RRAM operation.

We also observe in Figure 3.6(b) that while no apparent trend of R_{HRS} over the cycles can be seen, a stable and reproducible modulation of R_{LRS} by over one order of magnitude is achieved by varying I_{comp}, indicating the potential of using the single-crystal anatase TiO_2 material system for implementation of multilevel memory cells [79, 80]. Figure 3.6(c) shows R_{HRS} and R_{LRS} as a function of I_{comp} in the log R – log I form, summarizing the data from Figure 3.6(b). R_{HRS} is always above 10^{10} Ω over the entire range of I_{comp}, whereas R_{LRS} increases as I_{comp} decreases and eventually saturates at ~12.9 kΩ. It should be noted that in our measurements, the SET process does not occur for I_{comp} < 10 μA, from which we conclude that during the SET process a minimum compliance current is required to form and maintain a conductive nanofilament fully connecting the top and bottom electrodes. The saturation of R_{LRS} occurs at a resistance $R_0 = 1/G_0 = h/(2e^2)$, where h is Planck's constant and e is the magnitude of the electron charge. R_0 corresponds to the intrinsic contact resistance of a single-mode ballistic conductor sandwiched between two conductive contacts [101].

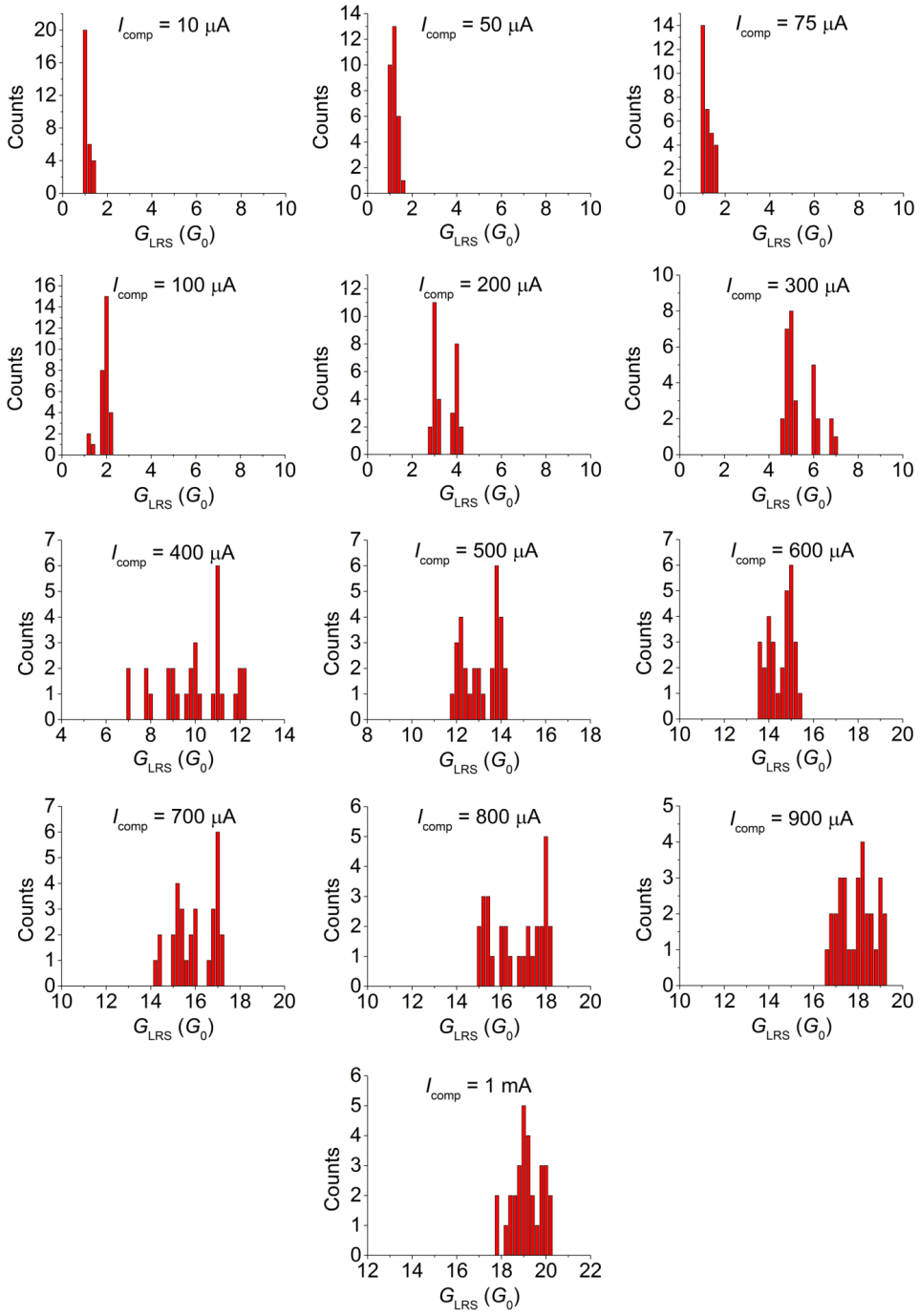
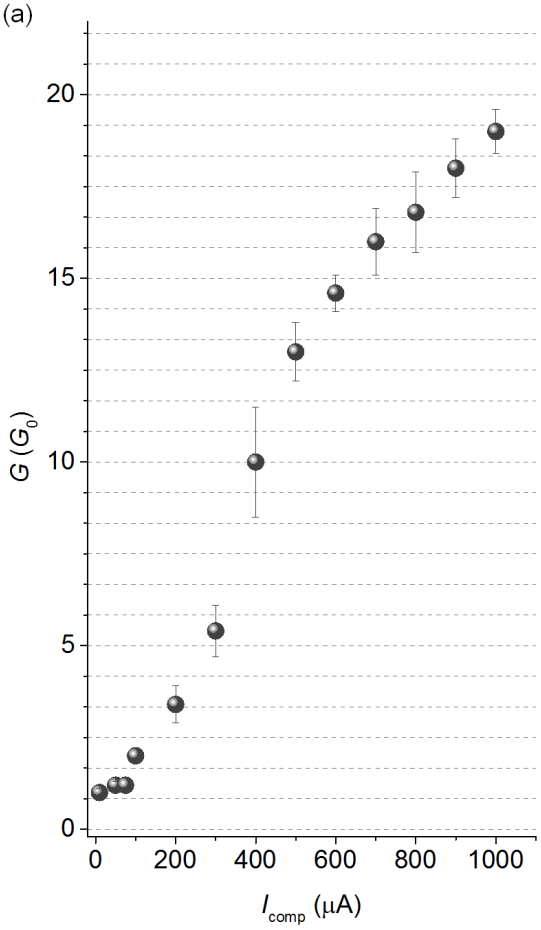

I_{comp} = 10 μA
I_{comp} = 50 μA
I_{comp} = 75 μA
I_{comp} = 100 μA
I_{comp} = 200 μA
I_{comp} = 300 μA
I_{comp} = 400 μA
I_{comp} = 500 μA
I_{comp} = 600 μA
I_{comp} = 700 μA
I_{comp} = 800 μA
I_{comp} = 900 μA
I_{comp} = 1 mA
Counts
G_{LRS} (G_0)

Figure 3.7.

Figure 3.7: Histograms of G_{LRS} in units of $G_0 = 2e^2/h$ for the 390 cycles (including the 100 successive cycles in Figure 3.6), with 30 cycles for each I_{comp}, showing effective modulation of the number of quantized channels by varying I_{comp}.

The quantized nature of conductance in the LRS is shown more explicitly in Figure 3.6(d), in which a histogram of the LRS conductance $G_{LRS} \equiv 1/R_{LRS}$ for the 100 successive cycles shown in Figure 3.6(b) reveals a series of discrete peaks around integer multiples of G_0. To further elucidate the role of I_{comp} in determining the number of conductance channels n, histograms of G_{LRS} in units of G_0 for 390 switching cycles (30 cycles for each I_{comp}) performed on the same TiO_2 device as that for Figure 3.6 are shown in Figure 3.7 for compliance currents up to 1 mA. At compliance currents of 10–200 μA, histogram peak(s) corresponding to one or two quantized conductance values for each I_{comp} can be seen, and the number of conductance channels n increases with I_{comp}. Within this range of compliance current (10–200 μA), G_{LRS} can be controlled to within a single quantum of conductance by imposing a given I_{comp} during the device SET process. Since G_{LRS} is extracted from linear I–V characteristics in the LRS, good control over n and therefore over the thickness of a conductive nanofilament at or near the atomic scale via I_{comp} is demonstrated. At all of the higher compliance currents tested (300 μA–1 mA), corresponding to larger numbers of conductance channels, n can be controlled to within $\pm(0.5–1.5)G_0$, with the average number of conductance channels increasing with I_{comp} and reaching $(19\pm0.6)G_0$ for I_{comp} = 1 mA. Figure 3.8(a) summarizes the data in Figure 3.7 by plotting G_{LRS} vs. I_{comp}, with the mean and standard deviation of G_{LRS} for each I_{comp} shown in Figure 3.8(b).

(a)



(b)

I_{comp} (μA)	Mean (G_0)	Std Dev (G_0)
10	1	0.1
50	1.2	0.1
75	1.2	0.2
100	2	0.2
200	3.4	0.5
300	5.4	0.7
400	10	1.5
500	13	0.8
600	14.6	0.5
700	16	0.9
800	16.8	1.1
900	18	0.8
1000	19	0.6

Figure 3.8: (a) G_{LRS} vs. I_{comp} for I_{comp} ranging from 10 μA to 1 mA summarized from each histogram in Fig. 6; (b) mean and standard deviation values of G_{LRS} in units of G_0 in (a).

The observation of highly controllable, reproducible QC raises the issue of the role the single-crystal anatase TiO_2 material system, including possible Magnéli-like nanophases, plays in demonstrating QC, and whether the observed QC with multiple quantized channels, i.e., for $n \geq 2$, corresponds to a single relatively thick nanofilament or a collection of independent thin nanofilaments [121, 122]. With regard to the first issue, it has been previously reported that Magnéli-like nanocolumns of 1–2 nm in width can exist with (101) crystallographic shear planes in thin epitaxial anatase TiO_2 films grown on

(001) $LaAlO_3$ planes [119], and that SET switching can be regarded as a local phase transformation of the TiO_2 film (anatase or rutile) to the Magnéli or Magnéli-like phase at the nanometer scale [78, 79, 95, 98]. It should be noted that R_{LRS} is essentially constant (with an increase by less than 1 Ω from 278 K to 338 K) around room temperature for each ON-state (e.g., Figure 3.4(b)), also indicating that electron transport through the metallic CF is ballistic, for which temperature-dependent scattering processes are generally absent. Therefore, the QC characteristics observed here in the LRS of the single-crystal anatase TiO_2 thin film are consistent with the localized formation of a filamentary quantized conductance channel consisting of a nanoscale Magnéli-like phase within which ballistic electron transport can occur. The bulk metal electrodes in contact with such a conductance channel could be either the Ti top and the n+ Si bottom electrodes, or thicker regions of metallic Magnéli-like phases that act as virtual metal electrodes connecting the atomic scale nanofilament to the Ti and n+ Si electrodes. In either case, the single-crystal nature and high quality of the anatase TiO_2 film is believed to play a key role in suppressing the background current and enabling the emergence of QC in the LRS.

With regard to the formation of a single filament or multiple filaments at high compliance currents, we see in Figure 3.3(b) that the CF is highly stable against further growth or rupturing at positive voltages once it is formed. In addition, it is widely known that regardless of the detailed RS mechanism, growth of a new CF is significantly suppressed after the cell is SET due to the combination of greatly decreased voltage drop across the cell upon SET and the exponential dependence of the CF growth rate on this voltage drop [79, 80]. Therefore, if a collection of independent nanofilaments were to account for the higher values of G_{LRS}, they would need to form essentially simultaneously at the SET voltage. In this case, however, it is very unlikely that there would be such a

clear monotonic dependence of n on I_{comp} (Figure 3.8), because the number of growing CFs before the cell is ON cannot be determined by I_{comp}. For $I_{comp} \geq 600$ μA, i.e., $n \geq 14$–16, the observed distribution of values for G_{LRS} begins to become more continuous, as shown in Figure 3.7. This can be understood as a consequence of the fact that for a thicker conductive nanofilament, the energy spacing between its subbands becomes smaller and eventually is comparable to or smaller than a few $k_B T$, in which case sharp transitions of conductance over adjacent n's are significantly smeared out [101]. This also suggests the formation of a single thick nanofilament with a large n instead of a collection of several independent thin nanofilaments with small n's. It is therefore highly likely that only a single thick nanofilament is formed for the cases where $n \geq 2$.

To help us further understand the resistive switching physics, the band diagram evolution of a complete switching process is depicted in Figure 3.9(a), based on the above qualitative conclusions drawn from the experimental results. During the electroforming/SET process, due to the upward growth of the aggregated oxygen vacancies, the conduction band of the metallic CF eventually extends from the bottom electrode to the top electrode, which increases the electric field in the gap between the top electrode and the CF tip, and accelerates the oxygen vacancy drift and therefore the SET process. Figures 3.9(b) and (c) show the HRS I-V characteristics from Figure 3.2(b), plotted as I-V^2 and $\ln(I/V)$-$V^{1/2}$, respectively. From Figure 3.9(b), I is found to be proportional to V^2 at voltages smaller than ~0.9 V in the HRS during the SET process, suggesting space charge limited current (SCLC) as the major transport mechanism within that voltage range. Since SCLC conduction occurs when the injected carrier density exceeds that of the thermally activated free carriers, the observation of very small SCLC-based current for low voltages is consistent with an extremely low concentration or low mobility of free carriers in the HRS, as expected in the presence of deep donor levels

associated with oxygen vacancies and/or Ti^{3+} interstitials. On the other hand, Poole-Frenkel emission is found to be the dominant transport process in the HRS for voltages higher than 0.9 V. As shown in Figure 3.9(c), the *I-V* relation observed in this voltage range is of the form

$$\frac{I}{V} \propto \exp\left[-\frac{q\left(\phi_B - \sqrt{qV/d_S \pi\varepsilon}\right)}{k_B T}\right] , \tag{3.1}$$

where q is the electron charge, ϕ_B the barrier height, ε the high-frequency dielectric constant of the insulator, d_S the gap size of the ruptured CF, k_B the Boltzmann constant, and T the absolute temperature. This behavior corresponds to that expected for Poole-Frenkel emission. Using Equation (3.1) and taking $\varepsilon = 8\varepsilon_o$ as the optical dielectric constant for anatase TiO_2 [123] where ε_o is the vacuum permittivity, we find that d_S averaged over the voltage range for which Poole-Frenkel emission dominates can be estimated from the slope shown in Figure 3.9(c) to be ~7 nm, which is close to the thickness of the TiO_2 layer. Poole-Frenkel emission, in which capture and emission of electrons by traps occurs by virtue of a lowered potential well along the direction of a high electric field, is prominent only when sufficient carriers and a sufficient density of traps are available, and its occurrence here is indicative of the efficient injection of electrons from the n+ Si substrate under a high electric field.

After the initial formation of the CF fully bridging the top and bottom electrodes, since most of the applied voltage still drops across the CF neck, the CF starts to expand laterally by the deposition of oxygen vacancies onto the lateral wall of the tapered CF neck, causing the electronic current through the structure to increase. At the point when the electronic current increases to the compliance current set by the instrument, an

internal current-limiting circuitry of the instrument starts to share the most part of the applied voltage, and the ionic current across the switching cell therefore becomes negligible. In this way, the lateral growth of the CF essentially stops, which defines R_{LRS} and stabilizes the CF conduction band that is shared with the top electrode.

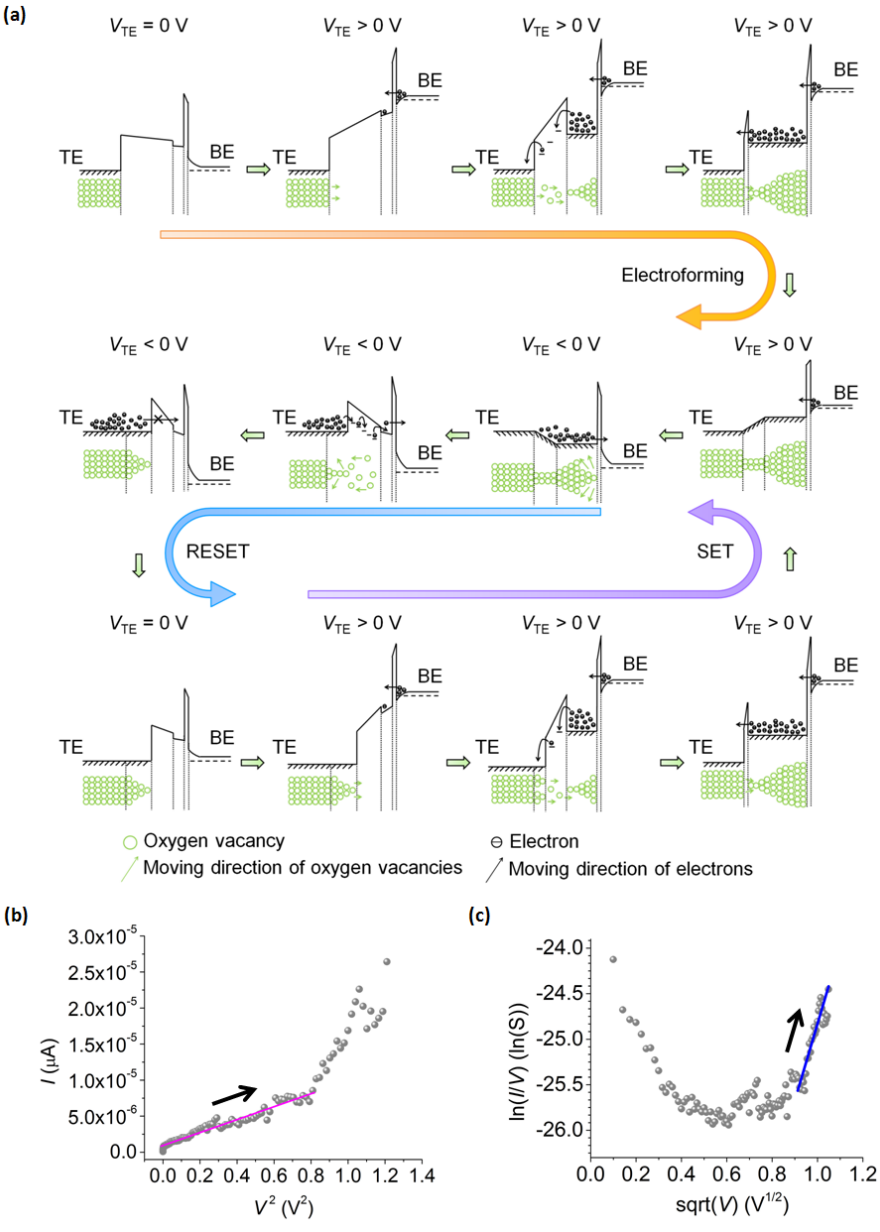


Figure 3.9.

Figure 3.9: (a) Band diagram evolution of a complete resistive switching process in the single-crystal TiO_2 materials system. TE and BE denote "top electrode" and "bottom electrode", respectively. (b) I-V^2 plot of the SET sweep before the device is on; (c) $\ln(I/V)$-$V^{1/2}$ version of (b).

Since there is effectively no compliance current applied during the RESET process, most of the bias voltage drops across the switching cell in the LRS. Due to the presence of the very thin SiO_x layer that separates the Si substrate from the active RS layer, an electron transfer overpotential difference builds up and enables electrochemical current across the SiO_x layer. Based on the same mechanism as that for the SET process, oxygen vacancies become oxidized again and dissolve starting from the part of the CF that is adjacent to the n+ Si bottom electrode. Once the bottom part of the CF fully dissolves, the CF ruptures and the cell is therefore switched off. Therefore, the total charge required to dissolve the bottom part of the CF determines the RESET characteristics such as V_{RESET} and I_{RESET}. Based on the Butler-Volmer equation responsible for electrochemical processes, it can be shown that V_{RESET} is only dependent on the volume and cross-sectional area of the bottom part of the CF. Since the CF neck close to the top electrode determines R_{LRS}, V_{RESET} is therefore independent of R_{LRS}, and I_{RESET} is inversely proportional to R_{LRS}, consistent with the experimental results shown in Figure 3.10.

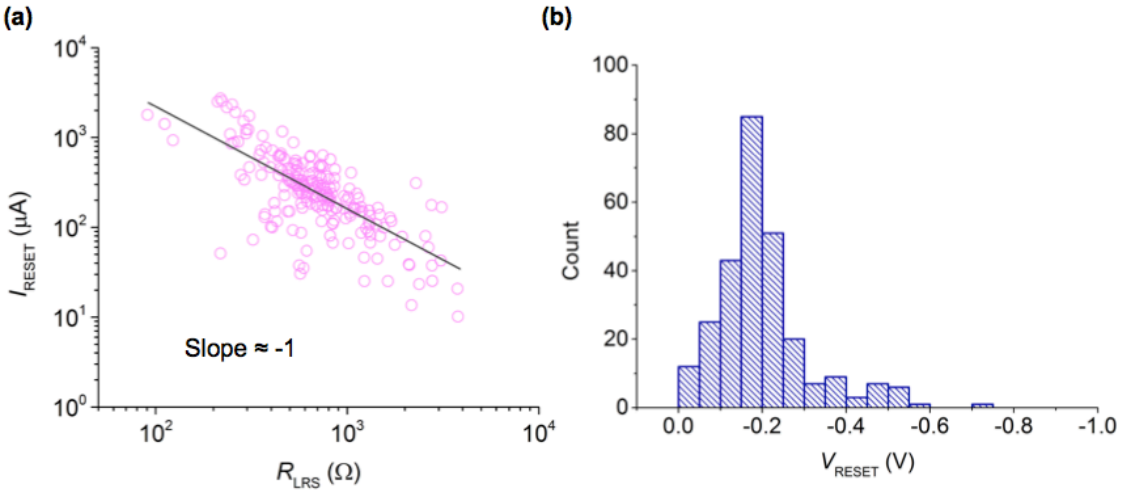


Figure 3.10.

Figure 3.10: (a) Scatter plot of I_{RESET} versus R_{LRS}. (b) Histogram of V_{RESET} that corresponds to the results shown in (a).

It is noteworthy that, as shown in Figure 3.8(a), G_{LRS} does not linearly vary with I_{comp} and instead increases faster with I_{comp} in the low compliance current regime (200 μA - 500 μA) than in the high compliance current (500 μA - 1 mA) and levels off in the ultra low compliance regime (10 μA - 100 μA). On the other hand, in a set of experiments performed on another device with the same layer structure, it is found that the voltage drop across the TiO_2 RRAM cell at the corresponding compliance current, labeled as V_C in Figure 3.2(b), increases linearly with $I_{comp}^{1/2}$ (Figure 3.11(a)), which equivalently means that G_{LRS} also increases linearly with $I_{comp}^{1/2}$. It should be noted that in most literature published so far, a constant V_C and therefore $G_{LRS} \propto I_{comp}$ are routinely observed as a "universal" phenomena [115], which contradicts with our observation from these single-crystal TiO_2 RRAM devices.

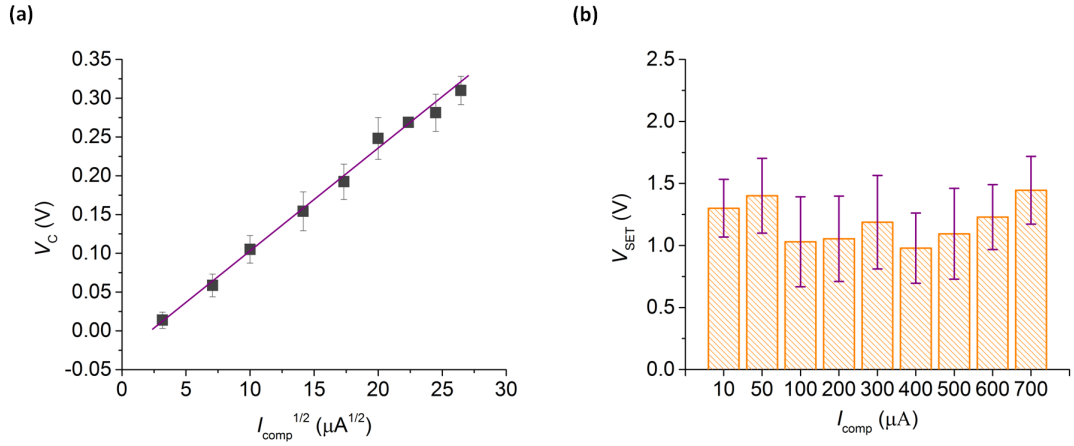


Figure 3.11: (a) The voltage drop across the TiO_2 RRAM cell at the corresponding compliance current, labeled as V_C in Figure 3.2(b), increases linearly with $I_{comp}^{1/2}$. Measurements were performed on an 8 nm TiO_2 RRAM device. (b) Histogram of V_{SET} vs. I_{comp} with 30 resistive switching processes for each I_{comp}.

To explain this behavior, we consider the lateral growth of a CF after the applied voltage reaches V_{SET} (i.e., after the initial completion of CF bridging) by using a

thermally-activated ion migration model [115, 124] and taking into account the tapered shape of the CF and ion distribution, which gives the lateral growth rate along one direction as follows [115],

$$\frac{dW_i}{dt} = Ae^{-\frac{E_{a0}-\alpha q V_{cell}}{k_B T_0\left(1+\frac{V_{cell}^2}{8T_0\rho k_{th}}\right)}} \frac{a_i}{R_j W_i} \quad , \tag{3.2}$$

where W_i denotes the length scale of the CF cross section in the i^{th} direction, a_i the lattice constant along the i^{th} direction of the CF cross section, R_j the aspect ratio of the CF on the j^{th} side of the cross section, A the growth rate constant, E_{a0} the activation energy of oxygen vacancy hopping, α the barrier lowering coefficient, V_{cell} the voltage drop across the device under test, k_B the Boltzmann constant, T_0 the room temperature 300 K, q the electronic charge, and ρ and k_{th} the resistivity and thermal conductivity of the CF, respectively. The model is then used in a numerical simulation with the application of a compliance current, a reasonable duration for filament growth during the switching and voltage sweep process that corresponds to the typical experimental condition, and the averaged experimental results on V_{SET} for each I_{comp} as shown in Figure 3.11(b). A schematic of the simulation model is shown in Figure 3.12(a), and the equivalent circuit and the voltage sweep scheme used in the model are shown in Figure 3.12(b) and (c), respectively. In the simulation, the parameters are set that $E_{A0} = 0.4$ eV, $\alpha = 0.5$, $A = 10^{-9}$ m/s, $k_{th} = 8$ W/(m K), $a_1 = a_2 = 0.5$ nm, and $R_1 = R_2 = 4$. It should be noted that the thermal conductivities for Si, TiO_2, SiO_2, Ti, and Au are known to be 149, 4.8–11.8, 1.4, 20, and 318 W/(m K), respectively. Therefore, the selection of 8 W/(m K) for the thermal conductivity of a conductive filament made of oxygen vacancies falls into a reasonable range of the possible value.

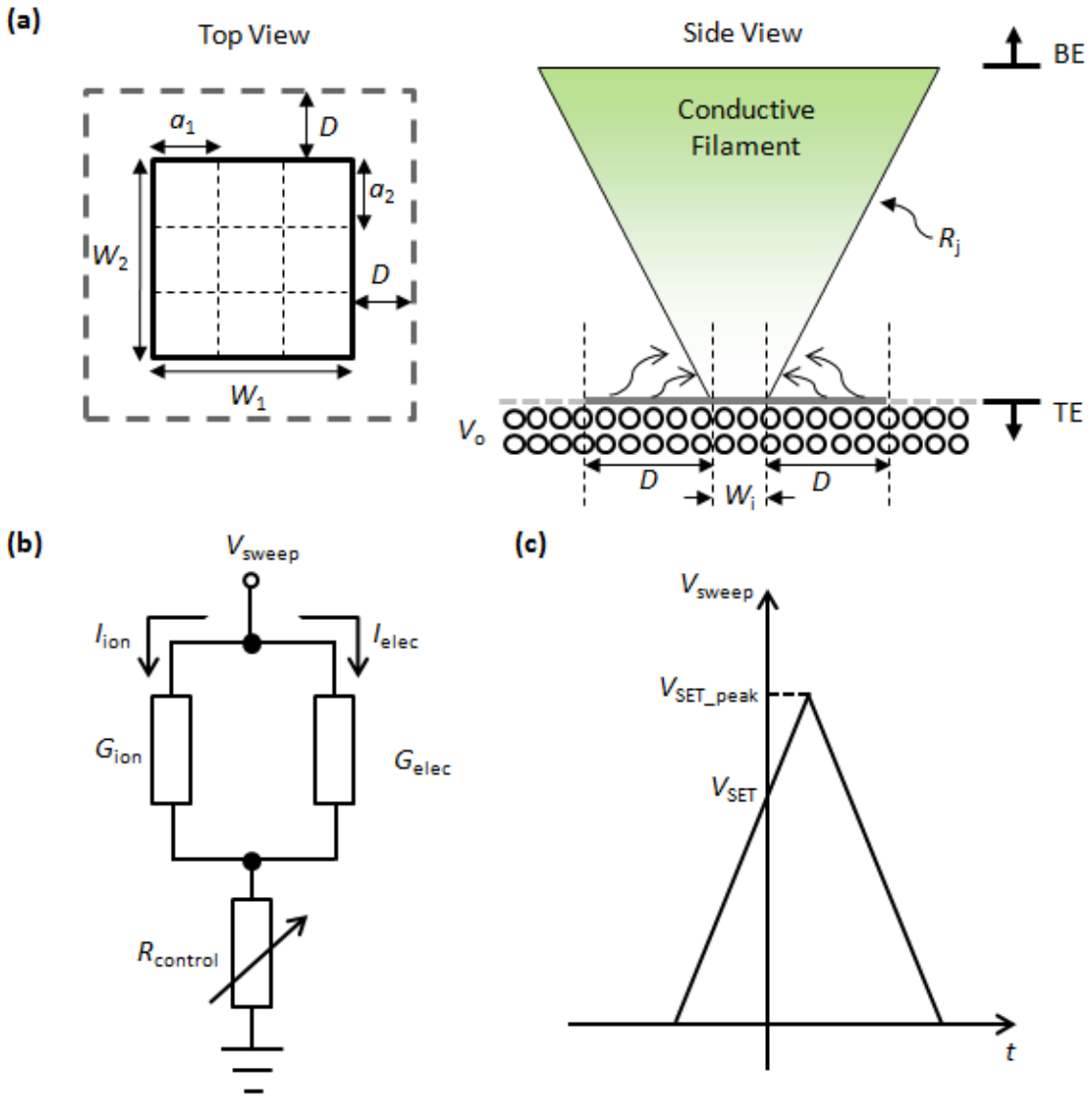


Figure 3.12: (a) Schematic (top view and side view) of the simulation model. (b) Equivalent circuit of the simulation model. (c) Voltage sweep scheme used in the simulation model that is consistent with the experimental condition.

Figure 3.13(a) shows the simulated and experimental results for G_{LRS} versus t for different compliance currents, from which good agreement can be seen. For a larger compliance current, G_{LRS} is larger and increases with t at a higher rate, indicating that I_{comp} sets the limit and rate for lateral expansion of the CF. As shown in Figures 3.13(b)-(d),

the time length after $V = V_{SET}$ for the SET process determines the functional relationship between G_{LRS} and I_{comp}. Specifically, t = 5 s leads to the saturating behavior of G_{LRS} vs. I_{comp}, t = 40 s leads to a square-root type of behavior, and t = 120 s recovers a linear relation as typically reported by other literature [115]. For all the cases, the leveling-off behavior at I_{comp} < 100 μA can be reproduced in the simulation. Since most of the lateral expansion occurs before the electronic current through the CF reaches I_{comp} and the initial cross section area of the fully-bridging CF defines the initial electronic current, the lateral expansion of the CF is very limited when I_{comp} falls below 100 μA, leading to the leveling-off behavior in the G_{LRS} vs. I_{comp} relationship. It should be noted that the model developed in this work is robust to small parameter variations.

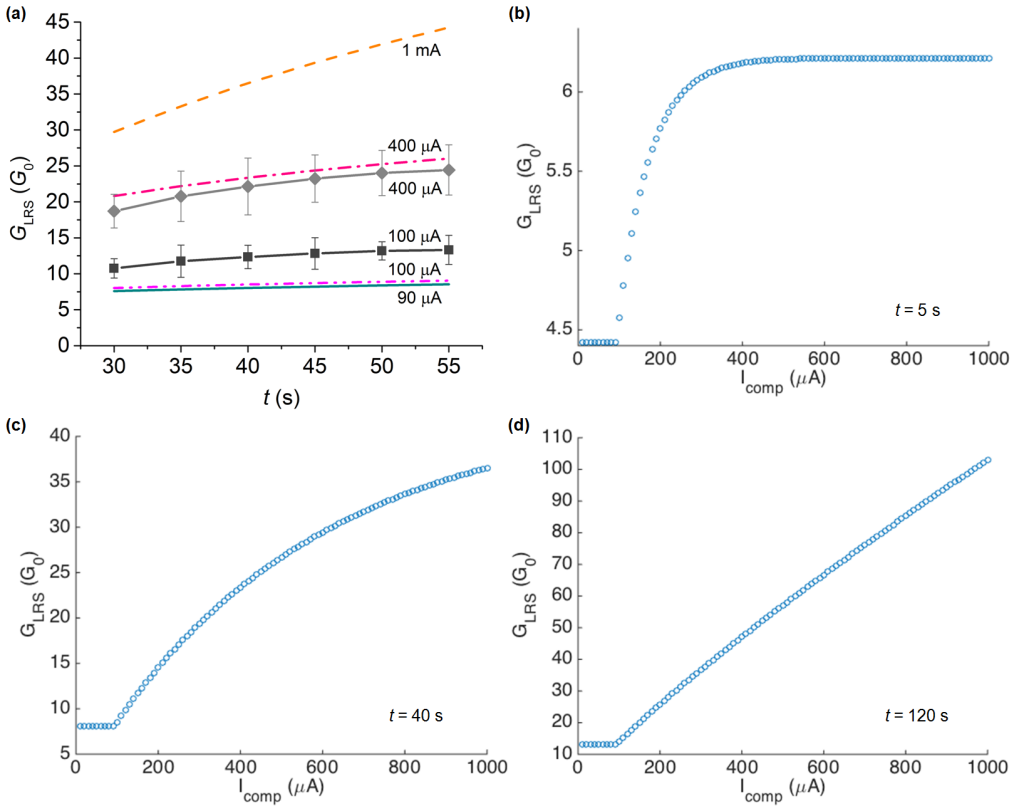


Figure 3.13.

Figure 3.13: (a) Simulation and experimental results on G_{LRS} versus t for different compliance currents (symbol-less curves for the simulation results and curves with symbols for the experimental results). Simulation results on G_{LRS} versus I_{comp} for (b) t = 5 s, (c) t = 40 s, and (d) t = 120 s.

The influence of different parameters in the model on G_{LRS} is shown in Figure 3.14. Figure 3.14(a) indicates that a small E_{a0} facilitates the oxygen vacancy hopping and leads to faster lateral expansion of the CF. As shown in Figure 3.14(b), a small k_{th} results in higher local temperature of the CF and assists in lateral expansion of the CF. With smaller aspect ratios, fewer oxygen vacancies are needed as building blocks for the CF expansion (Figure 3.14(c)). Figure 3.14(d) shows that a larger α brings better voltage control in lowering the potential barrier for oxygen vacancy hopping. It is noteworthy that general behaviors observed in our simulation are independent of details of the parameter values. The physics-based analytical model demonstrated here therefore justifies the proposed SET mechanism and recovers the experimentally observed V_c vs. I_{comp} and G_{LRS} vs. I_{comp} relations that are different from what have been reported in other literature. In addition, the physical model provides an explanation that justifies the voltage-polarity dependence of the BRS behavior and that reasonably describes the time-resolved electrochemical dissolution process for the CF during RESET.

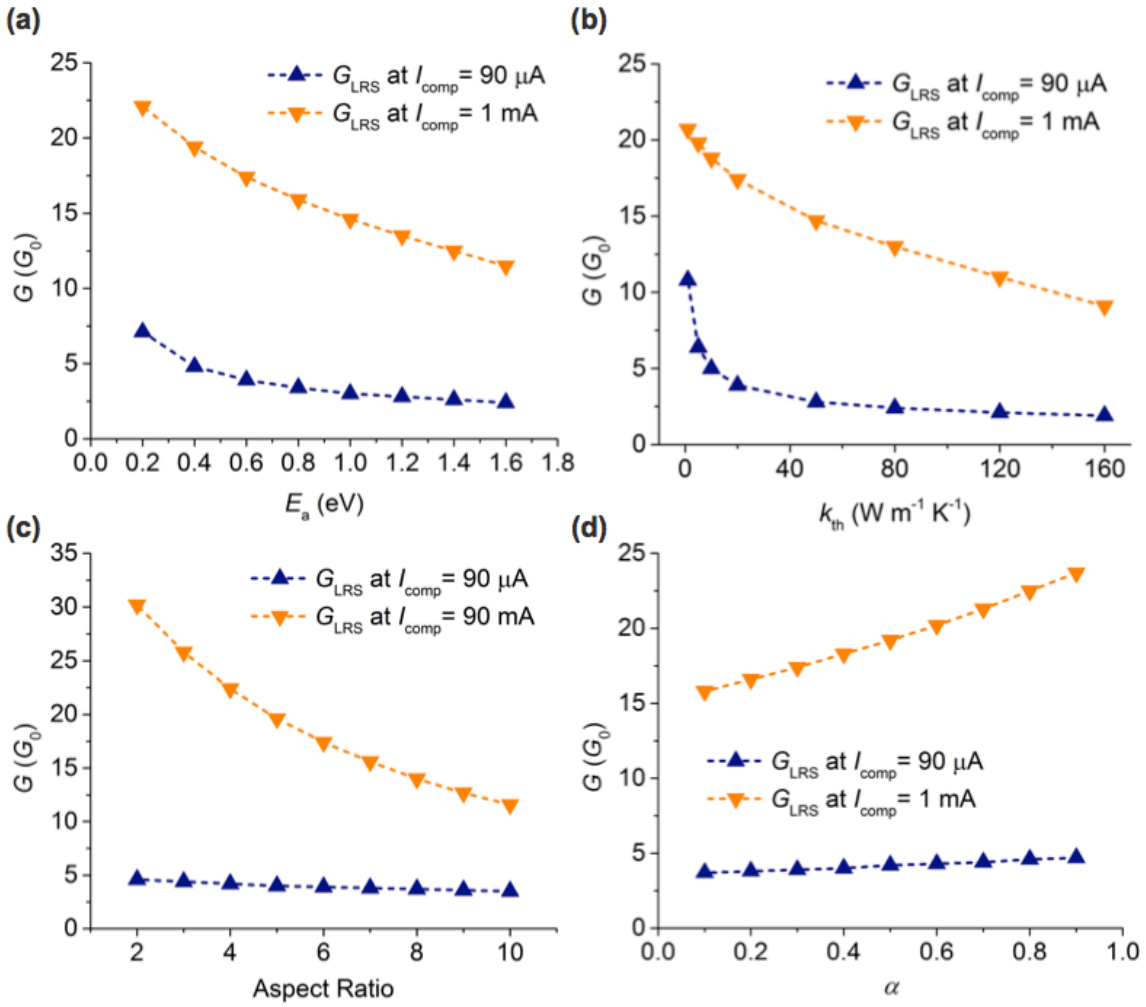


Figure 3.14: Simulation results for I_{comp} = 90 μA and I_{comp} = 1 mA on (a) G_{LRS} versus E_a, (b) G_{LRS} versus k_{th}, (c) G_{LRS} versus aspect ratio, and (d) G_{LRS} versus α.

3.4 SUMMARY

In this work, valence change-type BRS behavior observed in epitaxial single-crystal anatase TiO_2 thin film integrated on Si has been analyzed in detail, and highly controllable and reproducible quantized conductance has been demonstrated and analyzed. The electrical characteristics of the single-crystal anatase TiO_2 RRAM devices are shown to be very similar to those of electrochemical metallization rather than valence-change memory. Analysis of *I–V* characteristics reveals the metallic filamentary

nature of the LRS and that the filamentary-type valence-change effect is responsible for the observed RS behavior. Highly stable QC for R_{LRS} was observed, and shown to be highly controllable by varying the compliance current. In this manner, R_{LRS} can be precisely modulated over one order of magnitude, which is indicative of the potential of single-crystal anatase TiO_2 RRAM devices for scaling to atomic dimensions, and their potential suitability for implementation of approaches for increasing memory storage density using multilevel cells. We postulate that the single-crystal nature of the film plays a key role in suppressing the background current and therefore in the emergence of QC, and provide evidence that different values of QC are attained via control over the atomic-scale dimensions of single conducting filaments. A detailed and systematic analytical modeling is performed to reveal the resistive switching physics that accounts for our experimental results which are fundamentally different from what have been reported in other literature. These results suggest that single-crystal anatase TiO_2 films epitaxially grown on Si are particularly intriguing and promising as a platform for memory based on RS, and suggest a variety of directions for future explorations of performance, reliability, and scaling potential of these devices.

Chapter 4: Epitaxial $SrHfO_3$-Based Gate Dielectric Stacks for Germanium Metal-Oxide-Semiconductor Devices

4.1 INTRODUCTION

With recent advances in high-κ/metal-gate technology, [125] interest in germanium, an "old" semiconductor material, has resurged owing to its higher bulk electron and hole mobilities compared with those of silicon. [126–135] However, there remain several critical technical issues to be solved before Ge-channel MOSFETs can be integrated with mainstream Si complementary MOS technology. [126–135] An outstanding problem among these is the need for a high-quality and scalable gate dielectric on Ge. Unlike Si, the native oxide of Ge is thermally and chemically unstable and can readily decompose into several suboxides, potentially creating a high density of dangling bonds and a high degree of surface roughness at the GeO_x/Ge interface that act as scattering sources. [126, 128, 129, 132] These interfacial trap states, unfortunately, cannot be hydrogen passivated by using conventional forming gas anneals. [132]

Over the past few years, two approaches have proved successful to reduce interface trap density of Ge-based MOSFETs. The first employs a thin epitaxial Si passivation layer deposited on the Ge surface, which is then partially oxidized to form a tensile-strained Si/SiO_2 interfacial layer (IL). [126, 128] In such a way, the problem of Ge passivation is converted to the passivation of Si, which is much better understood. However, among several other issues, there exists an optimum Si cap thickness (~ 8 ML), which is limited by thickness-dependent strain relaxation of Si on Ge and Si oxidation as well as diffusion of Ge into the epitaxial Si layer. [128] The other approach uses a GeO_2 passivation layer on Ge, which can yield a mid-gap D_{it} as low as ~ 10^{11} cm^{-2} eV^{-1}. [128, 129] However, GeO_2 is water soluble and a H_2O-free gate-stack deposition process is needed. [128, 132] In addition, GeO_2 has a relative dielectric constant of 7, [132] and Ge

atoms can diffuse into the high-κ material if the GeO_2 IL is too thin. [126] These facts pose a great challenge for both approaches when it comes to scalability, [128] and intense research efforts are currently devoted to a search for alternative passivation layers or processing schemes. [135]

Concurrently, owing to the richness of their electronic, ionic, and magnetic properties, functional epitaxial binary oxides, perovskites, and oxide heterostructures have been under investigation for monolithic integration on mainstream semiconductor substrates such as Si (001) and Ge (001). [136] To date, a variety of functionalities such as magnetoresistance [17, 137–140], resistive switching [100, 141, 142], ferroelectricity [61, 143–146], and gate dielectrics [147, 148] have been achieved with epitaxial oxides integrated monolithically on Si (001). Moreover, in a report by McKee *et al.*, it has been shown that epitaxial oxides grown on Ge enable the formation of commensurate interface structures while maintaining continuity in dielectric displacement and systematic control of inversion charge, based on which a high-mobility MOSFET can be made. [6] Growth of single-crystal $SrTiO_3$ directly on Ge by ALD [149, 150] results in excellent crystallinity of the $SrTiO_3$ film as well as an abrupt $SrTiO_3$/Ge interface. [151] Although the $SrTiO_3$ film possesses a high dielectric constant, the negligible conduction band offset at the $SrTiO_3$/Ge interface [151] makes $SrTiO_3$ an inappropriate choice as the gate oxide for Ge-based MOSFETs. Unlike $SrTiO_3$, the large conduction band and valence band offsets of $SrHfO_3$ with Si and Ge enable it to be a promising candidate as a gate oxide material. [152–154] Recently, we reported the ALD growth and materials characterization of epitaxial $SrHfO_3$ on Ge with excellent crystallinity and favorable electronic properties as a high-κ oxide. [155] Here we report detailed analysis of several high-κ gate stacks composed of epitaxial crystalline $SrHfO_3$ grown directly on Ge by ALD, which show low leakage, small equivalent oxide thickness (EOT), and a reasonable

and improvable D_{it}. In contrast to GeO_2- or epitaxial Si-based passivation schemes, [126, 128] the high-κ gate-oxide stacks demonstrated here require no minimum thickness, making them highly promising for deep scaling.

4.2 Experimental Details

Metal-oxide-semiconductor (MOS) capacitors were created for three high-κ gate stack structures based on epitaxial $SrHfO_3$ grown directly on Ge by ALD. For each stack, amorphous $SrHfO_3$ films were deposited on the clean, 2×1 reconstructed Ge (001) surface at a substrate temperature of 225 °C using strontium bis(triisopropylcyclopentadienyl) [$Sr(^iPr_3Cp)_2$] (Absolut-Sr), hafnium formamidinate (Hf-FAMD), and purified water as co-reactants. The films were subsequently crystallized at temperatures between 650–725 °C in vacuum ($<2\times10^{-9}$ Torr) with a temperature ramp rate of 20 °C/min. The first gate stack consisted of a 4 nm $SrHfO_3$ film (referred to herein as the 4nm sample) that was crystallized by post-deposition vacuum annealing at 725 °C for 5 min. The second gate stack consisted of a 4 nm $SrHfO_3$ film capped with 2 nm of amorphous Al_2O_3 (referred to as the 4nm/2nm sample). In this case, the 4 nm $SrHfO_3$ film was grown in a two-step growth and anneal process, where 2 nm of $SrHfO_3$ were deposited each time and subsequently crystallized in vacuum at 700 °C for 5 min. In general, thinner $SrHfO_3$ films allowed for reduced annealing temperature for crystallization. For the third gate stack, 2 nm of $SrHfO_3$ was capped with 2 nm of amorphous Al_2O_3 (referred to as the 2nm/2nm sample). For this sample, the $SrHfO_3$ film was crystallized at 650 °C for 5 min, which was the lowest anneal temperature for which crystallization of the ALD-deposited $SrHfO_3$ layer was observed.

Figure 4.1(a) shows a schematic of the different gate stack structures for the 4nm sample, the 2nm/2nm sample, and the 4nm/2nm sample, respectively. Figures 4.1(b), (c)

and (d) show reflection high-energy electron diffraction (RHEED) images of the 4nm sample, the 2nm/2nm sample, and the 4nm/2nm sample, respectively, before deposition of the top amorphous Al_2O_3 layer (if any). For the 4nm/2nm sample, RHEED images taken after crystallization of the initially deposited 2 nm $SrHfO_3$ (upper two images) and after crystallization of the latter 2 nm $SrHfO_3$ (lower two images) are both shown in Figure 4.1(d). Streak patterns can be seen for all the three samples, indicative of the high crystalline quality of the $SrHfO_3$ film upon post-deposition annealing. Circular top electrode contacts with 15 μm radius were formed by sputtering of 200 nm TaN, photolithography, and SF_6-based inductive coupled plasma etching. The scratched backside of the n-type Ge substrate ($\rho \sim 0.029$–0.054 Ω cm) was coated with silver paste and then attached to a metal specimen disc. Electrical measurements were performed on a Cascade Microtech probe station in ambient conditions by applying voltage to the top electrode with the sample bottom grounded using an Agilent B1500A semiconductor device parameter analyzer.

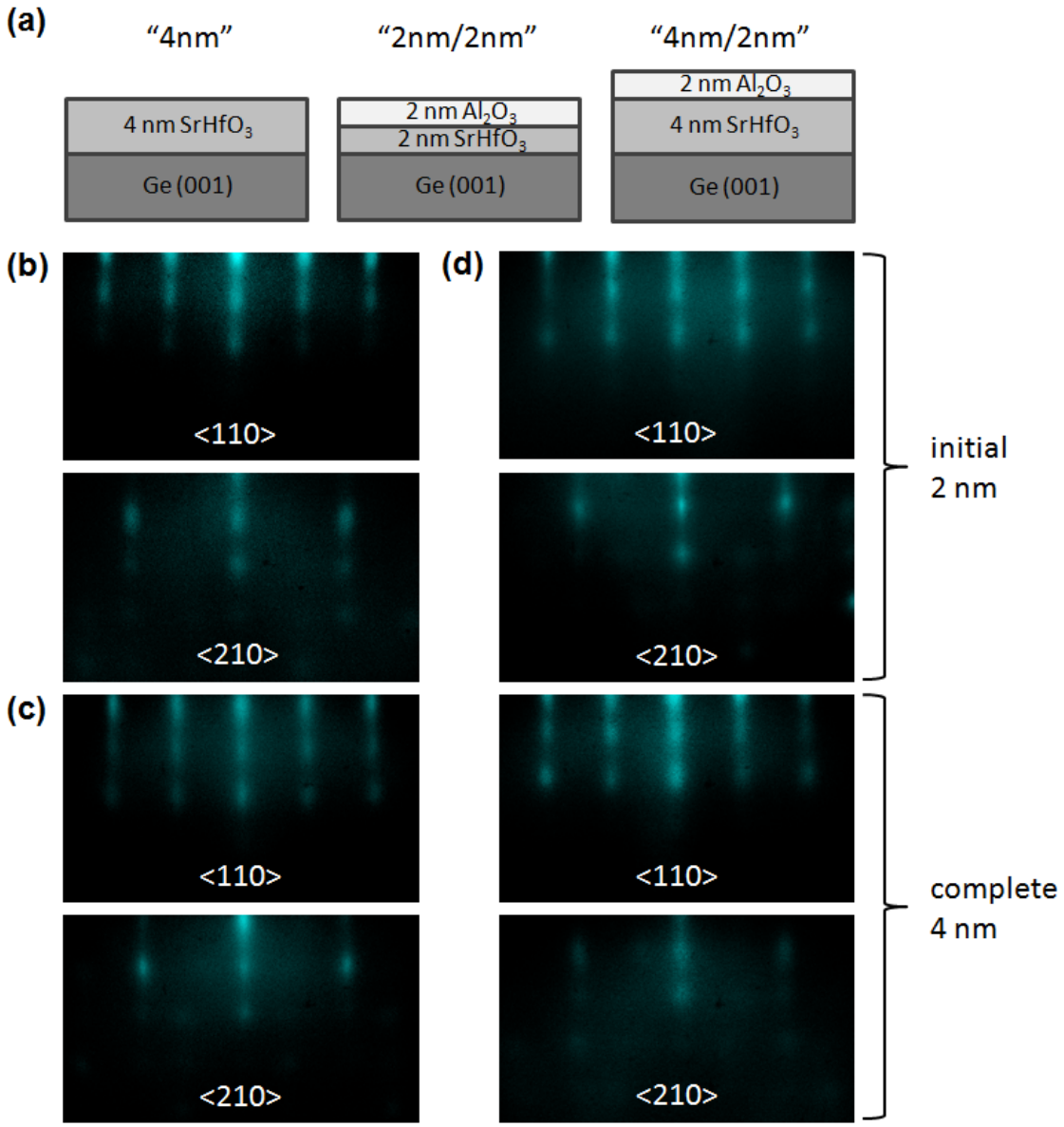


Figure 4.1: (a) Schematic diagrams of the 4nm, the 2nm/2nm, and the 4nm/2nm samples. Reflection high-energy electron diffraction images obtained from as-crystallized (b) 4 nm $SrHfO_3$ film for the 4nm sample, (c) 2 nm $SrHfO_3$ film for the 2nm/2nm sample, and (d) the initial 2 nm $SrHfO_3$ film (upper two images) and the complete 4 nm $SrHfO_3$ film (lower two images) for the 4nm/2nm sample. For each set of images taken, the beam is aligned along the [110] (top image) and the [210] (bottom image) azimuth.

4.3 RESULTS AND DISCUSSION

Figures 4.2(a) and (b) show the capacitance–voltage (*C–V*) and conductance–voltage (*G–V*) characteristics of the 4nm sample measured at frequencies ranging from 1 kHz to 1 MHz. The frequency dispersion of the *C–V* curves shows a clear signature of high-rate generation-recombination of minority carriers via midgap bulk traps in the Ge depletion layer (in the strong inversion regime) and via interface states (in the depletion and weak inversion regime), as well as a very short minority carrier response time, both due to the smaller band gap of Ge ($E_{g,Ge}$ = 0.67 eV) as compared to Si ($E_{g,Si}$ = 1.12 eV). [156, 157] This behavior is also indicated in the *G–V* curves shown in Figure 4.2(b), from which conductance plateaus in strong inversion and outstanding conductance peaks in depletion and weak inversion are observed. *C* increases as *V* becomes more negative in the strong inversion regime even at 1 MHz, suggesting impurity (e.g., hafnium atom) diffusion into the Ge substrate near the Ge/$SrHfO_3$ interface, which act as bulk traps assisting generation/recombination of minority carriers within the depletion layer in the strong inversion regime. [156]

Such behavior together with the large conductance plateaus in strong inversion was not seen for the 2nm/2nm sample and the 4nm/2nm sample, which were crystallized at lower temperatures. This indicates that crystallization temperature plays a significant role in the occurrence and degree of impurity diffusion from the gate dielectric to the Ge substrate, as also reflected in a comparison of the transmission electron microscopy images of these samples reported elsewhere. [155] Figure 4.2(c) shows that the dielectric leakage current of the 4nm sample scales almost linearly with the device area, indicating an area-distributed leakage current through the 4 nm $SrHfO_3$ layer rather than a localized one. An additional series of samples with different thicknesses (4.6 nm, 5.2 nm, 11.2 nm, and 18.2 nm) was grown with the same growth condition as that for the 4 nm $SrHfO_3$

sample to determine the dielectric constant of the $SrHfO_3$. Figure 4.2(d) shows the capacitance per unit area measured in the accumulation regime for different thicknesses of the crystallized $SrHfO_3$ film, from which a dielectric constant $\kappa = 16$ can be extracted, consistent with previous reports. [152, 154]

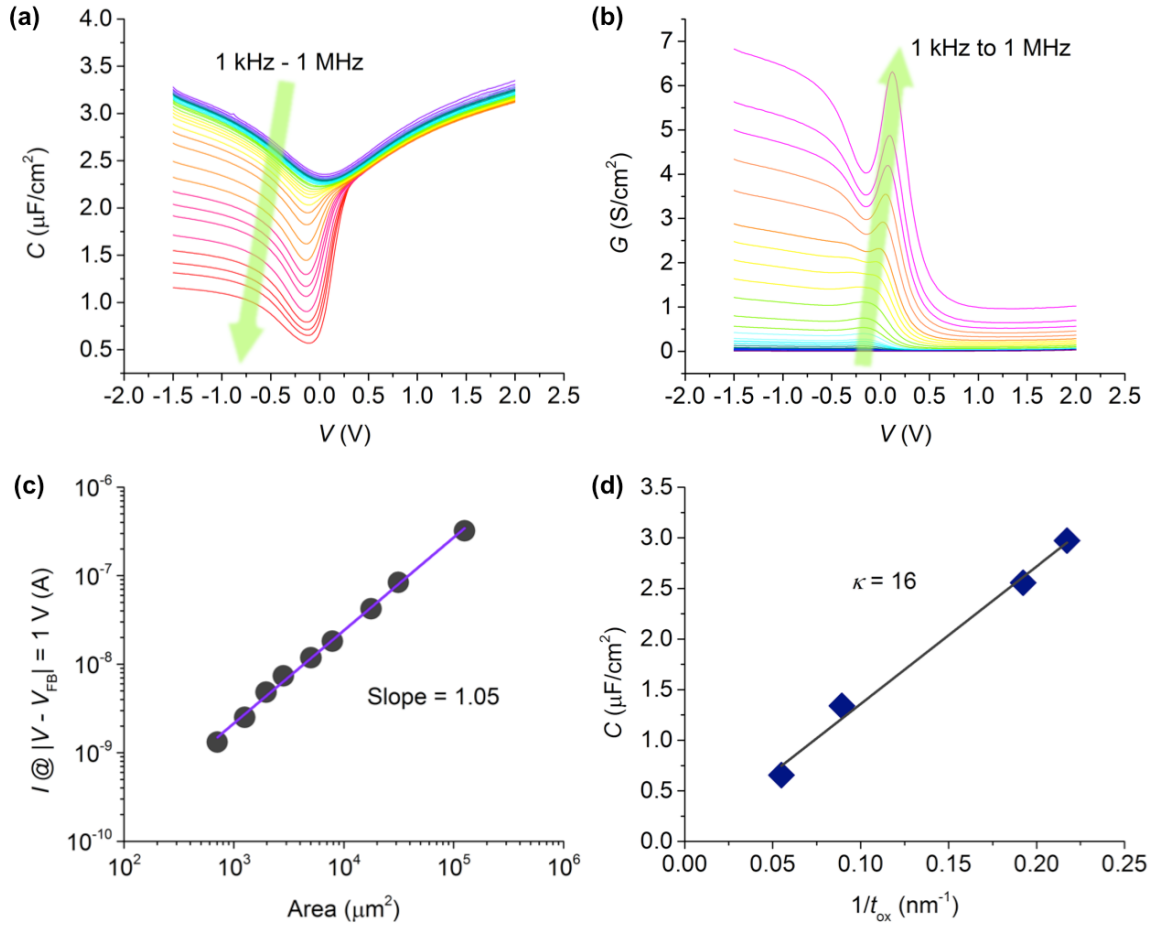


Figure 4.2: (a) Capacitance–voltage and (b) conductance–voltage characteristics of the 4nm sample for frequencies from 1 kHz to 1 MHz; (c) leakage current as a function of device area for the 4nm sample; (d) capacitance measured at 1 MHz in the accumulation regime for the $SrHfO_3$ films of different thickness for extraction of the dielectric constant of $SrHfO_3$.

Figures 4.3(a), (b) and (c) show the current density–voltage (*J–V*) characteristics for the 4nm, 2nm/2nm, and 4nm/2nm samples, respectively, all measured from the same

15 μm-radius devices used for *C–V* and *G–V* measurements, with their corresponding *C–V* curves obtained at 1 MHz shown in Figures 4.3(d), (e) and (f). The 2nm/2nm sample is more insulating than the 4nm sample, which can be understood by the fact that Al_2O_3 has a large band gap of 8.8 eV and a conduction band offset (CBO) of at least 2.6 eV with Ge, [158] whereas the $SrHfO_3$ has a band gap of 6.1 eV and a CBO of 2.17 eV with Ge. [155] As shown in Figure 4.3(c), the 4nm/2nm sample is the most insulating among the three samples, further verifying the high quality of the as-grown $SrHfO_3$ film. Note that the flattened *J–V* curves around 0 V shown in Figures 4.3(b) and (c) are due to the minimum current level detectable by the testing equipment for the 15 μm-radius devices, and therefore are likely to overestimate the leakage current for the corresponding voltage range. Nevertheless, the current densities shown in Figure 4.3 are well below the level required for these oxide stacks to be used as a gate dielectric.

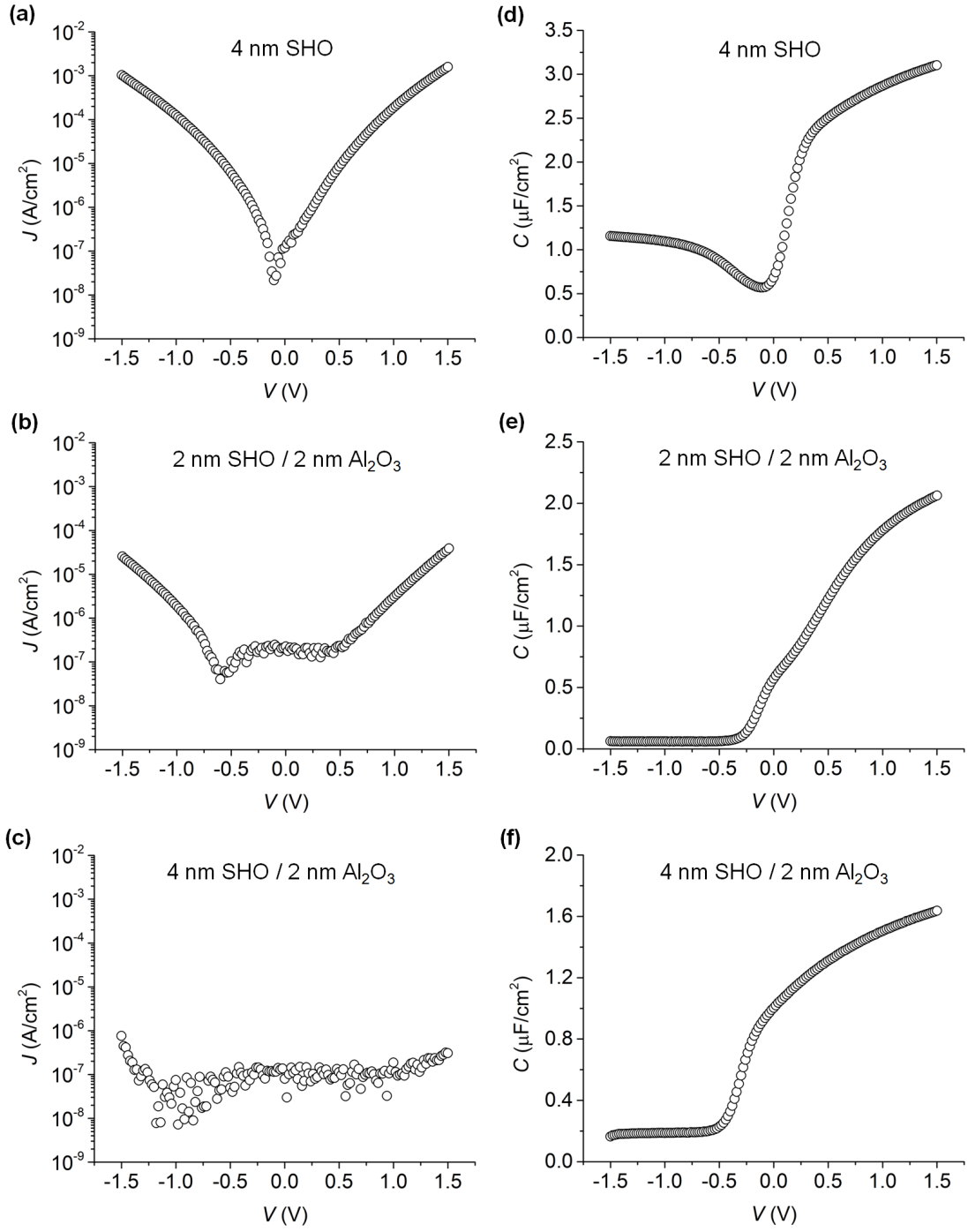


Figure 4.3: Leakage current density as a function of voltage for (a) the 4nm, (b) the 2nm/2nm, and (c) the 4nm/2nm samples, with their corresponding capacitance-voltage characteristics measured at 1 MHz shown in (d), (e), and (f), respectively.

The interface trap density D_{it} has also been extracted for all the samples under study using the conductance method. [159] Shown in Figure 4.4(a) are the parallel conductance loss peaks (G_p) in the frequency domain for the un-annealed 4nm/2nm sample as an example. Figure 4.4(b) shows the energy profile of D_{it} for the air-annealed 2nm/2nm sample. It should be noted that the energy dependence of D_{it} is similar for all the samples under study. For the samples with an Al_2O_3 capping layer, it is expected that the Al_2O_3 layer would not affect D_{it} due to the underlying $SrHfO_3$ layer, which is at least 2 nm thick. The un-annealed 4nm/2nm sample shows a midgap (minimum) D_{it} of 1.4×10^{13} cm^{-2} eV^{-1} (Figure 4.4(c)), much lower than that of the un-annealed 4nm sample (5.1×10^{13} cm^{-2} eV^{-1}, not shown). It is noteworthy that the crystallization temperature for the 4nm/2nm sample is 25 °C lower than the 4nm sample, reducing the possibility of intermixing at the $SrHfO_3$/Ge interface, [155] which is known to cause high D_{it}. [126–134] The improvement in D_{it} from the 4nm sample to the 4nm/2nm sample is believed to be related to the two-step growth technique, allowing for lower crystallization temperature to be adopted after $SrHfO_3$ growth of the 4nm/2nm stack. As shown in Figure 4.1, the RHEED images for the as-crystallized initial 2 nm $SrHfO_3$ (Figure 4.1(d)) show sharper lines than that of the one-step grown and as-crystallized 4 nm $SrHfO_3$ (Figure 4.1(b)), indicating that higher crystallinity (less disorder) can be achieved by annealing a thinner 2 nm $SrHfO_3$ film. The improvement in D_{it} with lower crystallization temperature can be further justified in Figure 4.4(c) through the comparison between the un-annealed 4nm/2nm sample and the un-annealed 2nm/2nm sample, for which the midgap D_{it} is 5.4×10^{12} cm^{-2} eV^{-1}, and for which the crystallization temperature is 50 °C lower than the former. Previous studies have indicated that lower annealing temperature may result in small, isolated amorphous regions in the $SrHfO_3$ film. [155] However, our measurements of the $SrHfO_3$ dielectric constant, shown in Figure 4.2(d), indicate that any

formation of such small and isolated amorphous regions that occurs here does not increase EOT, despite the fact that the dielectric constant of as-deposited amorphous $SrHfO_3$ is determined to be ~7 based on the *C–V* measurements (not shown).

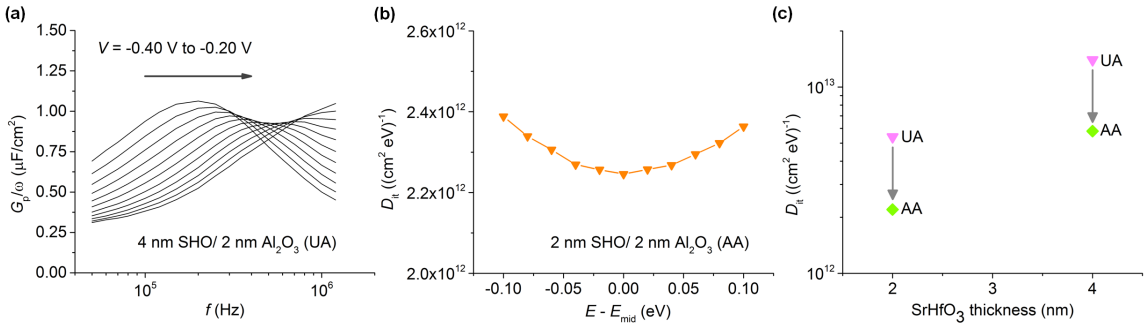


Figure 4.4: (a) Parallel conductance loss peaks in the frequency domain for the un-annealed 4nm/2nm sample; (b) Energy profile of interface trap density extracted for the air-annealed 2nm/2nm sample; (c) Midgap (minimum) interface trap density for the 4nm/2nm sample and 2nm/2nm sample before and after air-anneal. "UA" and "AA" denote "un-annealed" and "air-annealed", respectively.

The influence of additional annealing procedures on D_{it} has also been investigated. As indicated in Figure 4.4(c), 30 min annealing in air at 300 °C after the sample growth and before the device fabrication lowers D_{it} minimum for the 4nm/2nm sample and the 2nm/2nm sample to 5.8×10^{12} cm^{-2} eV^{-1} and 2.2×10^{12} cm^{-2} eV^{-1}, respectively, both by ~60%. While the air anneal is clearly very effective in reducing D_{it}, it was experimentally verified that other annealing schemes such as wet oxidation anneal or forming gas anneal at temperatures similar to 300 °C did not reduce D_{it} (not shown). It should also be noted that the air anneal performed in this work did not cause any significant degradation of EOT. Specifically, EOTs for the un-annealed 4nm, 2nm/2nm, and 4nm/2nm are 1 nm, 1.7 nm, and 2.1 nm, respectively, whereas EOTs for the air-annealed 4nm, 2nm/2nm, and 4nm/2nm are 1.1 nm, 1.6 nm, and 2.2 nm, respectively. To

further reduce D_{it}, the influence of chemical composition of the annealing atmosphere on D_{it} reduction and the physical mechanism of how the $SrHfO_3$/Ge interface is affected by air annealing need to be clarified. It is believed that D_{it} can be improved with further optimization of the annealing atmosphere and temperature.

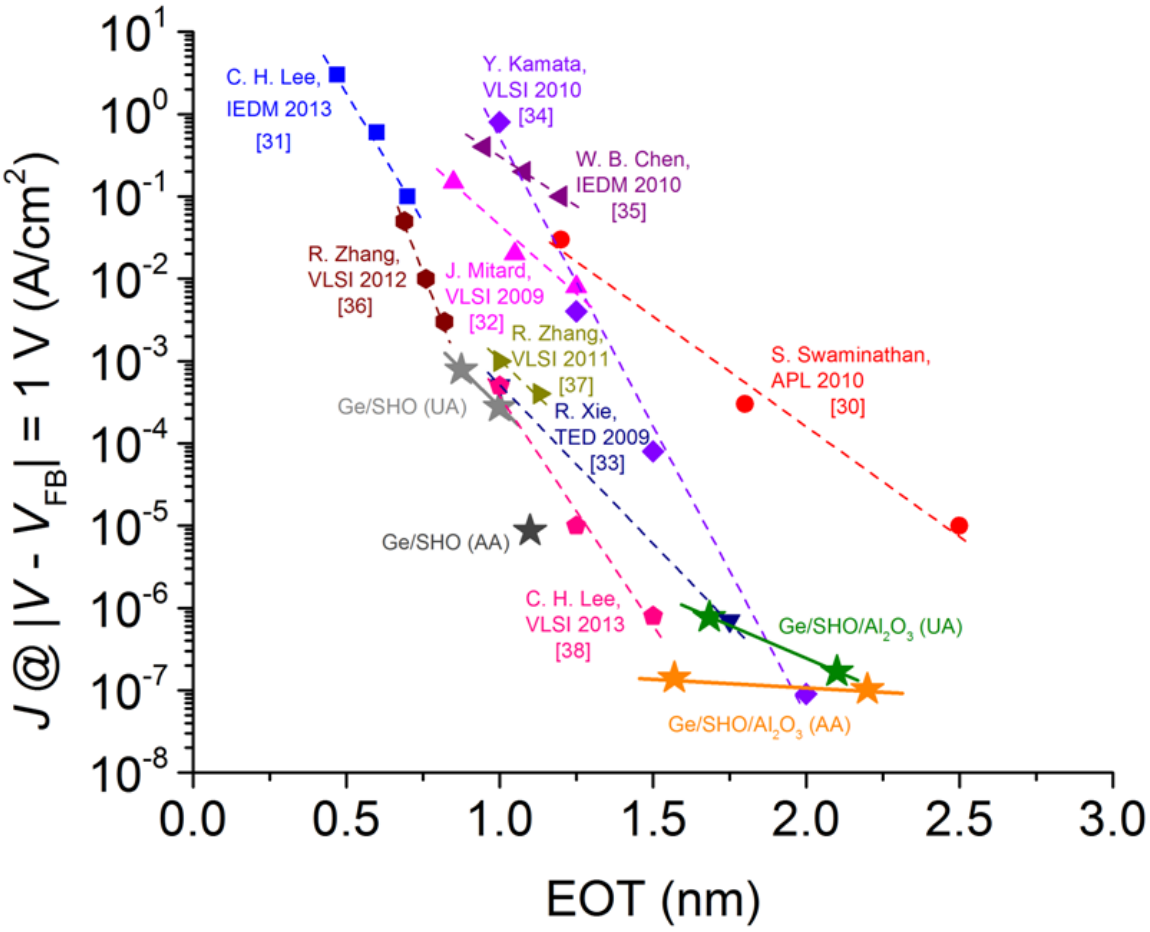


Figure 4.5: Leakage current versus EOT reported as the state of the art in recently published work together with our results in this work (star symbols). "UA" and "AA" denote "un-annealed" and "air-annealed", respectively.

Our results yield combinations of leakage current suppression and EOT that compare very favorably with the current state of the art. Figure 4.5 shows J vs. EOT found in recent reports that represent the state of the art of gate stack development for

Ge-based MOSFETs, [160–168] along with our results in this work (indicated by stars). Specifically, leakage currents measured for both the un-annealed and the air-annealed $SrHfO_3$ films or $SrHfO_3/Al_2O_3$ stacks in this work define the lower bound of J for their corresponding ranges of EOT in Figure 4.5, respectively. Moreover, with further scaling of the gate dielectric stacks, it is expected that the advantage of using the gate stacks developed in this work regarding the combination of J and EOT would be even more pronounced. It should also be noted that for the previous publications shown in Figure 4.5 that reported a D_{it} minimum, [160, 161, 163, 166–168] the D_{it}'s are mainly on the order of lower 10^{11} cm^{-2} eV^{-1}, which is about 10 times lower than the best D_{it} achieved in this work. Therefore, for our $SrHfO_3$-based gate stacks, a D_{it} comparable to the current state of the art remains to be achieved.

4.4 SUMMARY

In summary, we demonstrate the use of gate dielectric stacks based on ALD-grown epitaxial $SrHfO_3$ for Ge-based MOS applications. The gate stacks developed in this work yield combinations of ultralow leakage current and a small EOT which are comparable or superior to the state of the art published so far in the gate stack development for Ge-based MOSFETs. In addition, D_{it} has shown to be lowered by using (i) a two-step technique for the epitaxial growth; (ii) a lower crystallization temperature for minimized intermixing at the $SrHfO_3$/Ge interface; and (iii) post-growth air annealing. Findings of this work hold a great promise of using epitaxial gate dielectrics for Ge MOSFETs and suggest possible routes to further optimizing the electrical properties of these gate stacks.

Chapter 5: Summary and Outlook

5.1 SUMMARY

Metal oxides in epitaxial thin film form, enabled by recent advancements in materials growth techniques such as molecular beam epitaxy and atomic layer deposition, represent an important class of materials that can be monolithically integrated on mainstream semiconductor substrate materials and exhibit a wide variety of intriguing electronic, magnetic, optical, and chemical properties, many of which are unattainable with conventional semiconductor materials. With the introduction of epitaxial metal oxides, novel device functionalities can be achieved and incorporated into electronic components and systems with minimal impact on manufacturing compatibility with current semiconductor technologies. This dissertation demonstrates several device prototypes using epitaxial oxides as a key component, spanning from voltage-controlled ferromagnetism and magnetoresistance for sensing applications, to resistive random access memories for data storage, to gate dielectric stacks for logic technology.

Compared with their single-layer counterparts, epitaxial oxide heterostructures are expected to offer more degrees of freedom for integrating novel functionalities into conventional electronic devices and can even create exotic and unpredicted properties that cannot be achieved with a single oxide material. Here, we have designed, characterized, and analyzed devices based on $LaCoO_3/SrTiO_3$ heterostructures grown on Si (001) substrates by molecular beam epitaxy in which the combination of strain-dependent ferromagnetism in $LaCoO_3$, the converse piezoelectric effect in $SrTiO_3$, and strain coupling between these layers enables electrically controlled ferromagnetism and magnetoresistance to be achieved. Detailed mechanisms explaining this behavior are developed and verified using (i) the Valet-Fert model to quantify $LaCoO_3$ spin polarization, magnetic interfacial resistances, and the dependence of magnetoresistance

on device geometry; (ii) finite-element modeling of electric field distributions to explain variations in current transport for different gate finger geometries; and (iii) piezoresponse force microscopy studies to confirm the presence of piezoelectric response in $SrTiO_3$ films within our device structures. These results illustrate a new approach for electrically controlling local ferromagnetism in complex oxide heterostructures and for probing and controlling spin transport behavior in complex oxides at submicron dimensions, and offer the possibility of straightforward integration with conventional Si-based electronics via epitaxial growth directly on Si substrates.

TiO_2 is a prototypical platform and frontier for studies of oxygen vacancies and resistive memory development. It is believed that oxygen vacancies play a crucial role in driving resistive switching processes observed in TiO_2 material systems. Owing to the nearly perfect crystal structure and therefore minimized oxygen vacancy background in pristine devices, single-crystal epitaxial TiO_2 thin films can provide valuable information for revealing the physical nature of oxygen vacancy dynamics as being responsible for the resistive switching behavior, and are shown in this dissertation to exhibit switching characteristics that differ dramatically from those observed in other forms of TiO_2.

Here, valence change-type bipolar resistive switching behavior observed in epitaxial single-crystal anatase TiO_2 thin film integrated on Si has been analyzed in detail, and highly controllable and reproducible quantized conductance has been demonstrated and analyzed. The electrical characteristics of the single-crystal anatase TiO_2 resistive memory devices are shown to be very similar to those of electrochemical metallization rather than valence-change memory. Analysis of *I–V* characteristics reveals the metallic filamentary nature of the low resistance state and that the filamentary-type valence-change effect is responsible for the observed resistive switching behavior. Highly stable quantized conductance for R_{LRS} was observed, and shown to be highly controllable

by varying the compliance current. In this manner, R_{LRS} can be precisely modulated over one order of magnitude, which is indicative of the potential of single-crystal anatase TiO_2 resistive memory devices for scaling to atomic dimensions, and their potential suitability for implementation of approaches for increasing memory storage density using multilevel cells. We postulate that the single-crystal nature of the film plays a key role in suppressing the background current and therefore in the emergence of quantized conductance, and provide evidence that different values of quantized conductance are attained via control over the atomic-scale dimensions of single conducting filaments. A detailed and systematic analytical modeling is performed to reveal the resistive switching physics that accounts for our experimental results which are fundamentally different from what have been reported in other literature. These results suggest that single-crystal anatase TiO_2 films epitaxially grown on Si are particularly intriguing and promising as a platform for memory based on resistive switching.

Epitaxial oxides can also be promising candidates for application as gate dielectrics for Ge-based field-effect transistors, for which the development has been largely hampered by the poor quality gate dielectric/channel interface. In this dissertation, we demonstrate the use of gate dielectric stacks based on ALD-grown epitaxial $SrHfO_3$ for Ge-based MOS applications. The gate stacks developed in this work yield combinations of ultralow leakage current and a small EOT which are comparable or superior to the state of the art published so far in the gate stack development for Ge-based MOSFETs. In addition, D_{it} has shown to be lowered by using (i) a two-step technique for the epitaxial growth; (ii) a lower crystallization temperature for minimized intermixing at the $SrHfO_3$/Ge interface; and (iii) post-growth air annealing. Findings of this work hold a great promise of using epitaxial gate dielectrics for Ge MOSFETs and suggest possible routes to further optimizing the electrical properties of these gate stacks.

5.2 OUTLOOK

In this dissertation, voltage-controlled ferromagnetism and magnetoresistance in $LaCoO_3/SrTiO_3$ heterostructures are studied in detail in the dc regime, and it remains to be seen how fast the ferromagnetism of $LaCoO_3$ can be switched on and off by removal and application of a gate bias voltage, which is particularly important when such a device is to be integrated into circuits and systems. On the other hand, the influence of further scaling dimensions (e.g., finger widths and separation widths) on the device performance remains to be investigated, especially when the finger and separation widths are comparable to spin relaxation lengths in $LaCoO_3$. Finally, extension of these or related phenomena to operation at room temperature is likely to be essential for application in practical devices.

For the single-crystal TiO_2 resistive memory, voltage pulse measurements need to be performed to study its switching speed and the dependence of endurance and retention on pulse application schemes such as pulse widths, heights, and time intervals. Since the TiO_2 resistive memory demonstrates quantized conductance that suggests its great potential for scaling, it is also worthwhile to study resistive switching behaviors of nanoscale TiO_2 devices. This can be done by fabricating nanoscale Ti/Au pads as top contact and oxygen reservoir using e-beam lithography, nanoimprint, or other nanolithography techniques and by employing conductive atomic force microscopy for locating a selected device and performing electrical measurements.

Although the epitaxial $SrHfO_3$-based high-κ gate dielectric stacks show superior combinations of equivalent oxide thickness and gate leakage current over most published work, the interface trap density still needs to be significantly improved in order for the gate stacks developed in this dissertation to compete with the state of the art. Along this direction, *in situ* post-growth anneal in hydrogen or deuterium might help more

effectively passivate the oxide/Ge interface. Also, a more detailed theoretical and experimental investigation into the influence of air anneal on the interface trap reduction will help better understand the nature of interface traps and aid in optimizing the process integration flow that makes better use of epitaxial gate dielectrics.

References

[1] S. A. Chambers, *Adv. Mater.* **22**, 219–248 (2010).

[2] A. Ohtomo and H. Y. Hwang, *Nature* **427**, 423–426 (2004).

[3] C. A. F. Vaz, J. Hoffman, C. H. Ahn, and R. Ramesh, *Adv. Mater.* **22**, 2900–2918 (2010).

[4] M. V. Ganduglia-Pirovano, A. Hofmann, and J. Sauer, *Surf. Sci. Rep.* **62**, 219–270 (2007).

[5] K. Szot, M. Rogala, W. Speier, Z. Klusek, A. Besmehn, and R. Waser, *Nanotechnology* **22**, 254001 (2011).

[6] R. A. McKee, F. J. Walker, and M. F. Chisholm, *Science* **293**, 468–471 (2001).

[7] H. Y. Hwang, Y. Iwasa, M. Kawasaki, B. Keimer, N. Nagaosa, and Y. Tokura, *Nature Mater.* **11**, 103–113 (2012).

[8] J. Mannhart and D. G. Schlom, *Science* **327**, 1607–1611 (2010).

[9] M. Bibes, J. E. Villegas, and A. Barthélémy, *Adv. Phys.* **60**, 5–84 (2011).

[10] P. Zubko, S. Gariglio, M. Gabay, P. Ghosez, and J.-M. Triscone, *Annu. Rev. Condens. Matter Phys.* **2**, 141–165 (2011).

[11] J. M. Rondinelli and N. A. Spaldin, *Adv. Mater.* **23**, 3363–3381 (2011).

[12] C. H. Ahn, J.-M. Triscone, and J. Mannhart, *Nature* **424**, 1015–1018 (2003).

[13] P. Moetakef, J. R. Williams, D. G. Ouellette, A. P. Kajdos, D. Goldhaber-Gordon, S. J. Allen, and S. Stemmer, *Phys. Rev. X* **2**, 021014 (2012).

[14] Y. Xie, C. Bell, Y. Hikita, and H. Y. Hwang, *Adv. Mater.* **23**, 1744–1747 (2011).

[15] W. Eerenstein, N. D. Mathur, and J. F. Scott, *Nature* **442**, 759–765 (2006).

[16] S.-W. Cheong and M. Mostovoy, *Nature Mater.* **6**, 13–20 (2007).

[17] R. Ramesh and N. A. Spaldin, *Nature Mater.* **6**, 21–29 (2007).

[18] L. W. Martin, S. P. Crane, Y.-H. Chu, M. B. Holcomb, M. Gajek, M. Huijben, C.-H. Yang, N. Balke, and R. Ramesh, *J. Phys.: Condens. Matter* **20**, 434220 (2008).

[19] J. Wang, J. B. Neaton, H. Zheng, V. Nagarajan, S. B. Ogale, B. Liu, D. Viehland, V. Vaithyanathan, D. G. Schlom, U. V. Waghmare, N. A. Spaldin, K. M. Rabe, M. Wuttig, and R. Ramesh, *Science* **299**, 1719–1722 (2003).

[20] T. Zhao, A. Scholl, F. Zavaliche, K. Lee, M. Barry, A. Doran, M. P. Cruz, Y. H. Chu, C. Ederer, N. A. Spaldin, R. R. Das, D. M. Kim, S. H. Baek, C. B. Eom, and R. Ramesh, *Nature Mater.* **5**, 823–829 (2006).

[21] I. C. Infante, J. Juraszek, S. Fusil, B. Dupé, P. Gemeiner, O. Diéguez, F. Pailloux, S. Jouen, E. Jacquet, G. Geneste, J. Pacaud, J. Íñiguez, L. Bellaiche, A. Barthélémy, B. Dkhil, and M. Bibes, *Phys. Rev. Lett.* **107**, 237601 (2011).

[22] M. Ramazanoglu, M. Laver, W. Ratcliff, II, S. M. Watson, W. C. Chen, A. Jackson, K. Kothapalli, S. Lee, S.-W. Cheong, and V. Kiryukhin, *Phys. Rev. Lett.* **107**, 207206 (2011).

[23] N. Balke, S. Choudhury, S. Jesse, M. Huijben, Y. H. Chu, A. P. Baddorf, L. Q. Chen, R. Ramesh, and S. V. Kalinin, *Nat. Nanotechnol.* **4**, 868–875 (2009).

[24] S. H. Baek, H. W. Jang, C. M. Folkman, Y. L. Li, B. Winchester, J. X. Zhang, Q. He, Y. H. Chu, C. T. Nelson, M. S. Rzchowski, X. Q. Pan, R. Ramesh, L. Q. Chen, and C. B. Eom, *Nature Mater.* **9**, 309–314 (2010).
[25] A. Vasudevarao, A. Kumar, L. Tian, J. H. Haeni, Y. L. Li, C.-J. Eklund, Q. X. Jia, R. Uecker, P. Reiche, K. M. Rabe, L. Q. Chen, D. G. Schlom, and V. Gopalan, *Phys. Rev. Lett.* **97**, 257602 (2006).
[26] M. Gajek, M. Bibes, S. Fusil, K. Bouzehouane, J. Fontcuberta, A. Barthélémy, and A. Fert, *Nature Mater.* **6**, 296–302 (2007).
[27] W.-G. Wang, M. Li, S. Hageman, and C. L. Chien, *Nature Mater.* **11**, 64–68 (2011).
[28] D. Chiba, M. Sawicki, Y. Nishitani, Y. Nakatani, F. Matsukura, and H. Ohno, *Nature* **455**, 515–518 (2008).
[29] J. T. Heron, M. Trassin, K. Ashraf, M. Gajek, Q. He, S. Y. Yang, D. E. Nikonov, Y-H. Chu, S. Salahuddin, and R. Ramesh, *Phys. Rev. Lett.* **107**, 217202 (2011).
[30] L. W. Martin, Y.-H. Chu, M. B. Holcomb, M. Huijben, P. Yu, S.-J. Han, D. Lee, S. X. Wang, and R. Ramesh, *Nano Lett.* **8**, 2050–2055 (2008).
[31] J. Allibe, S. Fusil, K. Bouzehouane, C. Daumont, D. Sando, E. Jacquet, C. Deranlot, M. Bibes, and A. Barthélémy, *Nano Lett.* **12**, 1141–1145 (2012).
[32] H. Zheng, J. Wang, S. E. Lofland, Z. Ma, L. Mohaddes-Ardabili, T. Zhao, L. Salamanca-Riba, S. R. Shinde, S. B. Ogale, F. Bai, D. Viehland, Y. Jia, D. G. Schlom, M. Wuttig, A. Roytburd, and R. Ramesh, *Science* **303**, 661–663 (2004).
[33] F. Zavaliche, H. Zheng, L. Mohaddes-Ardabili, S. Y. Yang, Q. Zhan, P. Shafer, E. Reilly, R. Chopdekar, Y. Jia, P. Wright, D. G. Schlom, Y. Suzuki, and R. Ramesh, *Nano Lett.* **5**, 1793–1796 (2005).
[34] S. Zhang, Y. G. Zhao, P. S. Li, J. J. Yang, S. Rizwan, J. X. Zhang, J. Seidel, T. L. Qu, Y. J. Yang, Z. L. Luo, Q. He, T. Zou, Q. P. Chen, J. W. Wang, L. F. Yang, Y. Sun, Y. Z. Wu, X. Xiao, X. F. Jin, J. Huang, C. Gao, X. F. Han, and R. Ramesh, *Phys. Rev. Lett.* **108**, 137203 (2012).
[35] Y.-H. Chu, L. W. Martin, M. B. Holcomb, M. Gajek, S.-J. Han, Q. He, N. Balke, C.-H. Yang, D. Lee, W. Hu, Q. Zhan, P.-L. Yang, A. Fraile-Rodríguez, A. Scholl, S. X. Wang, and R. Ramesh, *Nature Mater.* **7**, 478–482 (2008).
[36] M. Liu, O. Obi, J. Lou, Y. Chen, Z. Cai, S. Stoute, M. Espanol, M. Lew, X. Situ, K. S. Ziemer, V. G. Harris, and N. X. Sun, *Adv. Funct. Mater.* **19**, 1826–1831 (2009).
[37] J. Lou, M. Liu, D. Reed, Y. Ren, and N. X. Sun, *Adv. Mater.* **21**, 4711–4715 (2009).
[38] X. Hong, A. Posadas, A. Lin, and C. H. Ahn, *Phys. Rev. B* **68**, 134415 (2003).
[39] C. A. F. Vaz, Y. Segal, J. Hoffman, R. D. Grober, F. J. Walker, and C. H. Ahn, *Appl. Phys. Lett.* **97**, 042506 (2010).
[40] H. J. A. Molegraaf, J. Hoffman, C. A. F. Vaz, S. Gariglio, D. van der Marel, C. H. Ahn, and J.-M. Triscone, *Adv. Mater.* **21**, 3470–3474 (2009).
[41] S. Valencia, A. Crassous, L. Bocher, V. Garcia, X. Moya, R. O. Cherifi, C. Deranlot, K. Bouzehouane, S. Fusil, A. Zobelli, A. Gloter, N. D. Mathur, A.

Gaupp, R. Abrudan, F. Radu, A. Barthélémy, and M. Bibes, *Nature Mater.* **10**, 753–758 (2011).
[42] L. Bocher, A. Gloter, A. Crassous, V. Garcia, K. March, A. Zobelli, S. Valencia, S. Enouz-Vedrenne, X. Moya, N. D. Marthur, C. Deranlot, S. Fusil, K. Bouzehouane, M. Bibes, A. Barthélémy, C. Colliex, and O. Stéphan, *Nano Lett.* **12**, 376–382 (2012).
[43] C. A. F. Vaz, *J. Phys.: Condens. Matter* **24**, 333201 (2012).
[44] M. Weisheit, S. Fähler, A. Marty, Y. Souche, C. Poinsignon, and D. Givord, *Science* **315**, 349 (2007).
[45] H. Ohno, D. Chiba, F. Matsukura, T. Omiya, E. Abe, T. Dietl, Y. Ohno, and K. Ohtani, *Nature* **408**, 944–946 (2000).
[46] D. Chiba, M. Yamanouchi, F. Matsukura, and H. Ohno, *Science* **301**, 943–945 (2003).
[47] D. Chiba, S. Fukami, K. Shimamura, N. Ishiwata, K. Kobayashi, and T. Ono, *Nature Mater.* **10**, 853–856 (2011).
[48] Y. Yamada, K. Ueno, T. Fukumura, H. T. Yuan, H. Shimotani, Y. Iwasa, L. Gu, S. Tsukimoto, Y. Ikuhara, and M. Kawasaki, *Science* **332**, 1065 (2011).
[49] W. Eerenstein, M. Wiora, J. L. Prieto, J. F. Scott, and N. D. Mathur, *Nature Mater.* **6**, 348–351 (2007).
[50] J. D. Burton and E. Y. Tsymbal, *Phys. Rev. B* **80**, 174406 (2009).
[51] D. Fuchs, C. Pinta, T. Schwarz, P. Schweiss, P. Nagel, S. Schuppler, R. Schneider, M. Merz, G. Roth, and H. v. Löhneysen, *Phys. Rev. B* **75**, 144402 (2007).
[52] A. Posadas, M. Berg, H. Seo, A. de Lozanne, A. A. Demkov, D. J. Smith, A. P. Kirk, D. Zhernokletov, and R. M. Wallace, *Appl. Phys. Lett.* **98**, 053104 (2011).
[53] G. E. Sterbinsky, P. J. Ryan, J.-W. Kim, E. Karapetrova, J. X. Ma, J. Shi, and J. C. Woicik, *Phys. Rev. B* **85**, 020403(R) (2012).
[54] H. Seo, A. Posadas, and A. A. Demkov, *Phys. Rev. B* **86**, 014430 (2012).
[55] D. Fuchs, E. Arac, C. Pinta, S. Schuppler, R. Schneider, and H. v. Löhneysen, *Phys. Rev. B* **77**, 014434 (2008).
[56] A. Herklotz, A. D. Rata, L. Schultz, and K. Dörr, *Phys. Rev. B* **79**, 092409 (2009).
[57] K. Dörr, O. Bilani-Zeneli, A. Herklotz, A.D. Rata, K. Boldyreva, J.-W. Kim, M.C. Dekker, K. Nenkov, L. Schultz, and M. Reibold, *Eur. Phys. J. B* **71**, 361–366 (2009).
[58] S. Park, P. Ryan, E. Karapetrova, J. W. Kim, J. X. Ma, J. Shi, J. W. Freeland, and W. Wu, *Appl. Phys. Lett.* **95**, 072508 (2009).
[59] D. E. Grupp and A. M. Goldman, *Science* **276**, 392 (1997).
[60] J. H. Haeni, P. Irvin, W. Chang, R. Uecker, P. Reiche, Y. L. Li, S. Choudhury, W. Tian, M. E. Hawley, B. Craigo, A. K. Tagantsev, X. Q. Pan, S. K. Streiffer, L. Q. Chen, S. W. Kirchoefer, J. Levy, and D. G. Schlom, *Nature* **430**, 758–761 (2004).
[61] M. P. Warusawithana, C. Cen, C. R. Sleasman, J. C. Woicik, Y. Li, L. F. Kourkoutis, J. A. Klug, H. Li, P. Ryan, L.-P. Wang, M. Bedzyk, D. A. Muller, L.-Q. Chen, J. Levy, and D. G. Schlom, *Science* **324**, 367–370 (2009).

[62] H. W. Jang, A. Kumar, S. Denev, M. D. Biegalski, P. Maksymovych, C. W. Bark, C. T. Nelson, C. M. Folkman, S. H. Baek, N. Balke, C. M. Brooks, D. A. Tenne, D. G. Schlom, L. Q. Chen, X. Q. Pan, S. V. Kalinin, V. Gopalan, and C. B. Eom, *Phys. Rev. Lett.* **104**, 197601 (2010).
[63] T. Valet and A. Fert, *Phys. Rev. B* **48**, 7099–7113 (1993).
[64] Y. Wei, X. Hu, Y. Liang, D. C. Jordan, B. Craigo, R. Droopad, Z. Yu, A. Demkov, J. L. Edwards, and W. J. Ooms, *J. Vac. Sci. Technol. B* **20**, 1402 (2002).
[65] A. A. Demkov and X. Zhang, *J. Appl. Phys.* **103**, 103710 (2008).
[66] M. Choi, A. Posadas, R. Dargis, C.-K. Shih, A. A. Demkov, D. H. Triyoso, N. D. Theodore, C. Dubourdieu, J. Bruley, and J. Jordan-Sweet, *J. Appl. Phys.* **111**, 064112 (2012).
[67] T.-W. Huang, Y.-S. Chang, G.-J. Chen, C.-C. Chung, and Y.-H. Chang, *J. Electrochem. Soc.* **154**, G244–G250 (2007).
[68] D. Fuchs, C. W. Schneider, R. Schneider, and H. Rietschel, *J. Appl. Phys.* **85**, 7362 (1999).
[69] M. L. Reinle-Schmitt, C. Cancellieri, D. Li, D. Fontaine, M. Medarde, E. Pomjakushina, C. W. Schneider, S. Gariglio, Ph. Ghosez, J.-M. Triscone, and P. R. Willmott, *Nat. Commun.* **3**, 932 (2012).
[70] E. Iguchi, K. Ueda, and W. H. Jung, *Phys. Rev. B* **54**,17431–17437 (1996).
[71] J. T. Devreese, *Ency. Appl. Phys.* **14**, 383–409 (1996).
[72] I. K. Naik and T. Y. Tien, *J. Phys. Chem. Solids* **39**, 311–315 (1978).
[73] D. Fuchs, L. Dieterle, E. Arac, R. Eder, P. Adelmann, V. Eyert, T. Kopp, R. Schneider, D. Gerthsen, and H. v. Löhneysen, *Phys. Rev. B* **79**, 024424 (2009).
[74] A. Gruverman, O. Auciello, and H. Tokumoto, *Annu. Rev. Mater. Sci.* **28**, 101–123 (1998).
[75] D. R. Penn and M. D. Stiles, *Phys. Rev. B* **72**, 212410 (2005).
[76] J. Bass, W. P. Pratt, and P. A. Schroeder, *Comments Condens. Matter Phys.* **18**, 223 (1998).
[77] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, *Proc. IEEE* **85**, 1248–1271 (1997).
[78] R. Waser and M. Aono, *Nature Mater.* **6**, 833–840 (2007).
[79] R. Waser, R. Dittmann, G. Staikov, and K. Szot, *Adv. Mater.* **21**, 2632–2663 (2009).
[80] H.-S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, and M.-J. Tsai, *Proc. IEEE* **100**, 1951–1970 (2012).
[81] S. K. Kim, K. M. Kim, D. S. Jeong, W. Jeon, K. J. Yoon, and C. S. Hwang, *J. Mater. Res.* **28**, 313–325 (2013).
[82] B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Waser, B. Reichenberg, and S. Tiedke, *J. Appl. Phys.* **98**, 033715 (2005).
[83] D. S. Jeong, H. Schroeder, U. Breuer, and R. Waser, *J. Appl. Phys.* **104**, 123716 (2008).
[84] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, and R. S. Williams, *Nature Nanotechnol.* **3**, 429–433 (2008).

[85] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, *Nature* **453**, 80–83 (2008).
[86] Y. V. Pershin and M. Di Ventra, *IEEE Trans. Circuits Syst. I, Reg. Papers* **57**, 1857–1864 (2010).
[87] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, *Nature* **464**, 873-876 (2010).
[88] K. M. Kim, D. S. Jeong, and C. S. Hwang, *Nanotechnology* **22**, 254002 (2011).
[89] K. M. Kim, B. J. Choi, Y. C. Shin, S. Choi, and C. S. Hwang, *Appl. Phys. Lett.* **91**, 012907 (2007).
[90] K. M. Kim, B. J. Choi, M. H. Lee, G. H. Kim, S. J. Song, J. Y. Seok, J. H. Yoon, S. Han, and C. S. Hwang, *Nanotechnology* **22**, 254010 (2011).
[91] D. S. Jeong, H. Schroeder, and R. Waser, *Electrochem. Solid-State Lett.* **10**, G51–G53 (2007).
[92] S.-J. Park, J.-P. Lee, J. S. Jang, H. Rhu, H. Yu, B. Y. You, C. S. Kim, K. J. Kim, Y. J. Cho, S. Baik, and W. Lee, *Nanotechnology* **24**, 295202 (2013).
[93] K. M. Kim, G. H. Kim, S. J. Song, J. Y. Seok, M. H. Lee, J. H. Yoon, and C. S. Hwang, *Nanotechnology* **21**, 305203 (2010).
[94] S. Kim, H. Y. Jeong, S. K. Kim, S.-Y. Choi, and K. J. Lee, *Nano Lett.* **11**, 5438–5442 (2011).
[95] S. J. Song, J. Y. Seok, J. H. Yoon, K. M. Kim, G. H. Kim, M. H. Lee, and C. S. Hwang, *Sci. Rep.* **3**, 3443 (2013).
[96] S.-G. Park, B. Magyari-Köpe, and Y. Nishi, *IEEE Electron Device Lett.* **32**, 197–199 (2011).
[97] K. Kamiya, M. Y. Yang, S.-G. Park, B. Magyari-Köpe, Y. Nishi, M. Niwa, and K. Shiraishi, *Appl. Phys. Lett.* **100**, 073502 (2012).
[98] D.-H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X.-S. Li, G.-S. Park, B. Lee, S. Han, M. Kim, and C. S. Hwang, *Nature Nanotechnol.* **5**, 148–153 (2010).
[99] J. P. Strachan, M. D. Pickett, J. J. Yang, S. Aloni, A. L. D. Kilcoyne, G. Medeiros-Ribeiro, and R. S. Williams, *Adv. Mater.* **22**, 3573–3577 (2010).
[100] C. Hu, M. D. McDaniel, J. G. Ekerdt, and E. T. Yu, *IEEE Electron Device Lett.* **34**, 1385–1387 (2013).
[101] S. Datta, *Electronic Transport in Mesoscopic Systems* (Cambridge University Press), 1997.
[102] K. Terabe, T. Hasegawa, T. Nakayama, and M. Aono, *Nature* **433**, 47–50 (2005).
[103] S. Tappertzhofen, I. Valov, and R. Waser, *Nanotechnology* **23**, 145703 (2012).
[104] T. Hasegawa, K. Terabe, T. Tsuruoka, and M. Aono, *Adv. Mater.* **24**, 252–267 (2012).
[105] X. Zhu, W. Su, Y. Liu, B. Hu, L. Pan, W. Lu, J. Zhang, and R.-W. Li, *Adv. Mater.* **24**, 3941–3946 (2012).
[106] C. Chen, S. Gao, F. Zeng, G. Y. Wang, S. Z. Li, C. Song, and F. Pan, *Appl. Phys. Lett.* **103**, 043510 (2013).

[107] A. Mehonic, A. Vrajitoarea, S. Cueff, S. Hudziak, H. Howe, C. Labbé, R. Rizk, M. Pepper, and A. J. Kenyon, *Sci. Rep.* **3**, 2708 (2013).
[108] S. Long, X. Lian, C. Cagli, X. Cartoixà, R. Rurali, E. Miranda, D. Jiménez, L. Perniola, M. Liu, and J. Suñé, *Appl. Phys. Lett.* **102**, 183505 (2013).
[109] E. Miranda, A. Mehonic, J. Suñé, and A. J. Kenyon, *Appl. Phys. Lett.* **103**, 222904 (2013).
[110] S. Long, L. Perniola, C. Cagli, J. Buckley, X. Lian, E. Miranda, F. Pan, M. Liu, and J. Suñé, *Sci. Rep.* **3**, 2929 (2013).
[111] J. T. Mayer, U. Diebold, T. E. Madey, and E. Garfunkel, *J. Electron. Spectrosc. Relat. Phenom.* **73**, 1–11 (1995).
[112] A. Agrawal, J. Lin, B. Zheng, S. Sharma, S. Chopra, K. Wang, A. Gelatos, S. Mohney, and S. Datta, *VLSIT Tech. Dig.* T200–T201 (2013).
[113] M. D. McDaniel, A. Posadas, T. Q. Ngo, A. Dhamdhere, D. J. Smith, A. A. Demkov, and J. G. Ekerdt, *J. Vac. Sci. Technol. B* **30**, 04E111 (2012).
[114] D. Ielmini, F. Nardi, and C. Cagli, *IEEE Trans. Electron Devices* **58**, 3246–3253 (2011).
[115] D. Ielmini, *IEEE Trans. Electron Devices* **58**, 4309–4317 (2011).
[116] D. Ielmini, *IEDM Tech. Dig.* 409–412 (2011).
[117] I. Valov, R. Waser, J. R. Jameson, and M. N. Kozicki, *Nanotechnology* **22**, 254003 (2011).
[118] H.-S. P. Wong, S. Raoux, S. B. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, M. Asheghi, and K. E. Goodson, *Proc. IEEE* **98**, 2201–2227 (2010).
[119] R. Ciancio, E. Carlino, G. Rossi, C. Aruta, U. Scotti di Uccio, A. Vittadini, and A. Selloni, *Phys. Rev. B* **86**, 104110 (2012).
[120] I. Valov, E. Linn, S. Tappertzhofen, S. Schmelzer, J. van den Hurk, F. Lentz, and R. Waser, *Nat. Commun.* **4**, 1771 (2013).
[121] T. Ohno, T. Hasegawa, T. Tsuruoka, K. Terabe, J. K. Gimzewski, and M. Aono, *Nat. Mater.* **10**, 591–595 (2011).
[122] I. Valov, I. Sapezanskaia, A. Nayak, T. Tsuruoka, T. Bredow, T. Hasegawa, G. Staikov, M. Aono, and R. Waser, *Nat. Mater.* **11**, 530–535 (2012).
[123] D. Mardare and G. I. J. Rusu, *J. Optoelectron. Adv. M.* **3**, 95–100 (2001).
[124] U. Russo, D. Kamalanathan, D. Ielmini, A. L. Lacaita, and M. N. Kozicki, *IEEE Trans. Electron Devices* **56**, 1040–1047 (2009).
[125] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, *IEEE Electron Device Lett.* **25**, 408–410 (2004).
[126] P. S. Goley and M. K. Hudait, *Materials* **7**, 2301–2339 (2014).
[127] C. Claeys, J. Mitard, G. Hellings, G. Eneman, B. De Jaeger, L. Witters, R. Loo, A. Delabie, S. Sioncke, M. Caymax, and E. Simoen, *ECS Trans.* **54**, 25–37 (2013).
[128] E. Simoen, J. Mitard, G. Hellings, G. Eneman, B. De Jaeger, L. Witters, B. Vincent, R. Loo, A. Delabie, S. Sioncke, M. Caymax, and C. Claeys, *Mater. Sci. Semicond. Process.* **15**, 588–600 (2012).
[129] R. Pillarisetty, *Nature* **479**, 324–328 (2011).

[130] A. Toriumi, C. H. Lee, S. K. Wang, T. Tabata, M. Yoshida, D. D. Zhao, T. Nishimura, K. Kita, and K. Nagashio, *Tech. Dig. – Int. Electron Devices Meet.* **2011**, 646–649.
[131] M. Caymax, G. Eneman, F. Bellenger, C. Merckling, A. Delabie, G. Wang, R. Loo, E. Simoen, J. Mitard, B. De Jaeger, G. Hellings, K. De Meyer, M. Meuris, and M. Heyns, *Tech. Dig. – Int. Electron Devices Meet.* **2009**, 461–464.
[132] Y. Kamata, "High-*k*/Ge MOSFETs for future nanoelectronics," *Mater. Today* **11**, 30–38 (2008).
[133] D. P. Brunco, B. De Jaeger, G. Eneman, J. Mitard, G. Hellings, A. Satta, V. Terzieva, L. Souriau, F. E. Leys, G. Pourtois, M. Houssa, G. Winderickx, E. Vrancken, S. Sioncke, K. Opsomer, G. Nicholas, M. Caymax, A. Stesmans, J. Van Steenbergen, P. W. Mertens, M. Meuris, and M. M. Heyns, *J. Electrochem. Soc.* **155**, H552–H561 (2008).
[134] H. Shang, M. M. Frank, E. P. Gusev, J. O. Chu, S. W. Bedell, K. W. Guarini, and M. Leong, *IBM J. Res. & Dev.* **50**, 377–386 (2006).
[135] S. Gupta, X. Gong, R. Zhang, Y.-C. Yeo, S. Takagi, and K. C. Saraswat, *MRS Bull.* **39**, 678–686 (2014).
[136] A. A. Demkov, A. B. Posadas, H. Seo, M. Choi, K. J. Kormondy, P. Ponath, R. C. Hatch, M. D. McDaniel, T. Q. Ngo, and J. G. Ekerdt, *ECS Trans.* **54**, 255–269 (2013).
[137] J.-H. Kim, S. I. Khartsev, and A. M. Grishin, *Appl. Phys. Lett.* **82**, 4295–4297 (2003).
[138] A. K. Pradhan, S. Mohanty, K. Zhang, J. B. Dadson, E. M. Jackson, D. Hunter, R. R. Rakhimov, G. B. Loutts, J. Zhang, and D. J. Sellmyer, *Appl. Phys. Lett.* **86**, 012503 (2005).
[139] L. W. Martin, Y.-H. Chu, Q. Zhan, R. Ramesh, S.-J. Han, S. X. Wang, M. Warusawithana, and D. G. Schlom, *Appl. Phys. Lett.* **91**, 172513 (2007).
[140] C. Hu, K. W. Park, A. Posadas, J. L. Jordan-Sweet, A. A. Demkov, and E. T. Yu, *J. Appl. Phys.* **114**, 183909 (2013).
[141] C. Hu, M. D. McDaniel, A. Posadas, A. A. Demkov, J. G. Ekerdt, and E. T. Yu, *Nano Lett.* **14**, 4360–4367 (2014).
[142] E. T. Yu, C. Hu, M. D. McDaniel, A. Posadas, A. A. Demkov, and J. G. Ekerdt, *ECS Trans.* **64**, 147–152 (2014).
[143] C. H. Ahn, K. M. Rabe, and J.-M. Triscone, *Science* **303**, 488–491 (2004).
[144] Y. Wang, C. Ganpule, B. T. Liu, H. Li, K. Mori, B. Hill, M. Wuttig, R. Ramesh, J. Finder, Z. Yu, R. Droopad, and K. Eisenbeiser, *Appl. Phys. Lett.* **80**, 97–99 (2002).
[145] H. N. Lee, D. Hesse, N. Zakharov, and U. Gösele, *Science* **296**, 2006–2009 (2002).
[146] C. Dubourdieu, J. Bruley, T. M. Arruda, A. Posadas, J. Jordan-Sweet, M. M. Frank, E. Cartier, D. J. Frank, S. V. Kalinin, A. A. Demkov, and V. Narayanan, *Nature Nanotech.* **8**, 748–754 (2013).

[147] Z. Yu, J. Ramdani, J. A. Curless, C. D. Overgaard, J. M. Finder, R. Droopad, K. W. Eisenbeiser, J. A. Hallmark, W. J. Ooms, and V. S. Kaushik, *J. Vac. Sci. Technol. B* **18**, 2139 (2000).
[148] T. Q. Ngo, A. B. Posadas, M. D. McDaniel, C. Hu, J. Bruley, E. T. Yu, A. A. Demkov, and J. G. Ekerdt, *Appl. Phys. Lett.* **104**, 082910 (2014).
[149] M. Leskelä and M. Ritala, *Thin Solid Films* **409**, 138–146 (2002).
[150] S. M. George, *Chem. Rev.* **110**, 111–131 (2010).
[151] M. D. McDaniel, T. Q. Ngo, A. Posadas, C. Hu, S. Lu, D. J. Smith, E. T. Yu, A. A. Demkov, and J. G. Ekerdt, *Adv. Mater. Inter.* **1**, 1400081 (2014).
[152] C. Rossel, B. Mereu, C. Marchiori, D. Caimi, M. Sousa, A. Guiller, H. Siegwart, R. Germann, J.-P. Locquet, J. Fompeyrine, D. J. Webb, Ch. Dieker, and J. W. Seo, *Appl. Phys. Lett.* **89**, 053506 (2006).
[153] M. Sousa, C. Rossel, C. Marchiori, H. Siegwart, D. Caimi, J.-P. Locquet, D. J. Webb, R. Germann, J. Fompeyrine, K. Babich, J. W. Seo, and Ch. Dieker, *J. Appl. Phys.* **102**, 104103 (2007).
[154] C. Rossel, M. Sousa, C. Marchiori, J. Fompeyrine, D. Webb, D. Caimi, B. Mereu, A. Ispas, J. P. Locquet, H. Siegwart, R. Germann, A. Tapponnier, and K. Babich, *Microelectron. Eng.* **84**, 1869–1873 (2007).
[155] M. D. McDaniel, C. Hu, S. Lu, T. Q. Ngo, A. Posadas, A. Jiang, D. J. Smith, E. T. Yu, A. A. Demkov, and J. G. Ekerdt, *J. Appl. Phys.* **117**, 054101 (2015).
[156] P. Batude, X. Garros, L. Clavelier, C. Le Royer, J. M. Hartmann, V. Loup, P. Besson, L. Vandroux, Y. Campidelli, S. Deleonibus, and F. Boulanger, *J. Appl. Phys.* **102**, 034514 (2007).
[157] K. Martens, C. O. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes, and G. Groeseneken, *IEEE Trans. Electron Devices* **55**, 547–556 (2008).
[158] J. Robertson, *J. Vac. Sci. Technol. B* **18**, 1785–1791 (2000).
[159] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley, 1982.
[160] S. Swaminathan, M. Shandalov, Y. Oshima, and P. C. Mclntyre, *Appl. Phys. Lett.* **96**, 082904 (2010).
[161] C. H. Lee, C. Lu, T. Tabata, W. F. Zhang, T. Nishimura, K. Nagashio, and A. Toriumi, *Tech. Dig. – Int. Electron Devices Meet.* **2013**, 40–43.
[162] J. Mitard, C. Shea, B. DeJaeger, A. Pristera, G. Wang, M. Houssa, G. Eneman, G. Hellings, W-E. Wang, J. C. Lin, F. E. Leys, R. Loo, G. Winderickx, E. Vrancken, A. Stesmans, K. DeMeyer, M. Caymax, L. Pantisano, M. Meuris, and M. Heyns, *Tech. Dig. – VLSI Symp. Technol.* **2009**, 82–83.
[163] R. Xie, T. H. Phung, W. He, M. Yu, and C. Zhu, *IEEE Trans. Electron Devices* **56**, 1330–1337 (2009).
[164] Y. Kamata, K. Ikeda, Y. Kamimuta, and T. Tezuka, *Tech. Dig. – VLSI Symp. Technol.* **2010**, 211–212.
[165] W. B. Chen, B. S. Shie, A. Chin, K. C. Hsu, and C. C. Chi, *Tech. Dig. – Int. Electron Devices Meet.* **2010**, 420–423.

[166] R. Zhang, P. C. Huang, N. Taoka, M. Takenaka, and S. Takagi, *Tech. Dig. – VLSI Symp. Technol.* **2012**, 161–162.
[167] R. Zhang, T. Iwasaki, N. Taoka, M. Takenaka, and S. Takagi, *Tech. Dig. – VLSI Symp. Technol.* **2011**, 56–57.
[168] C. H. Lee, C. Lu, T. Tabata, T. Nishimura, K. Nagashio, and A. Toriumi, *Tech. Dig. – VLSI Symp. Technol.* **2013**, 28–29.

Vita

Son of a Professor of Chinese History, Chengqing Hu was born in Shanghai, China in 1986 and was raised on the campus of East China Normal University. He received his B.S. degree in Microelectronics from Fudan University in 2009, and started his graduate studies at the University of Texas at Austin in the same year, from which he received his M.S.E. and Ph.D. degrees in Electrical and Computer Engineering in May 2011 and in August 2015, respectively. Since May 2010, following a one-year teaching assistantship at the Department of Electrical and Computer Engineering, he has conducted research on the design, modeling, process integration, characterization, and analysis of novel electronic device prototypes using epitaxial oxides under the supervision of Professor Edward T. Yu at the Microelectronics Research Center. He is a member of IEEE, and has served as a reviewer for several academic journals, including Applied Physics Letters and IEEE Transactions on Nanotechnology.

Permanent email: chengqing@utexas.edu

This dissertation was typed by Chengqing Hu.